

Starload Schematics

Skylake-U

2016-02-18


REV : A00

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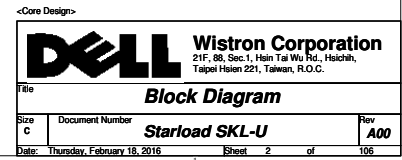
DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Variant Name>		
 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Cover Page		
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Star lord SKL-U Block Diagram




Main Func = CPU

(Blanking)

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(Reserved)

Size

A3

Document Number

Starload SKL-U

Rev

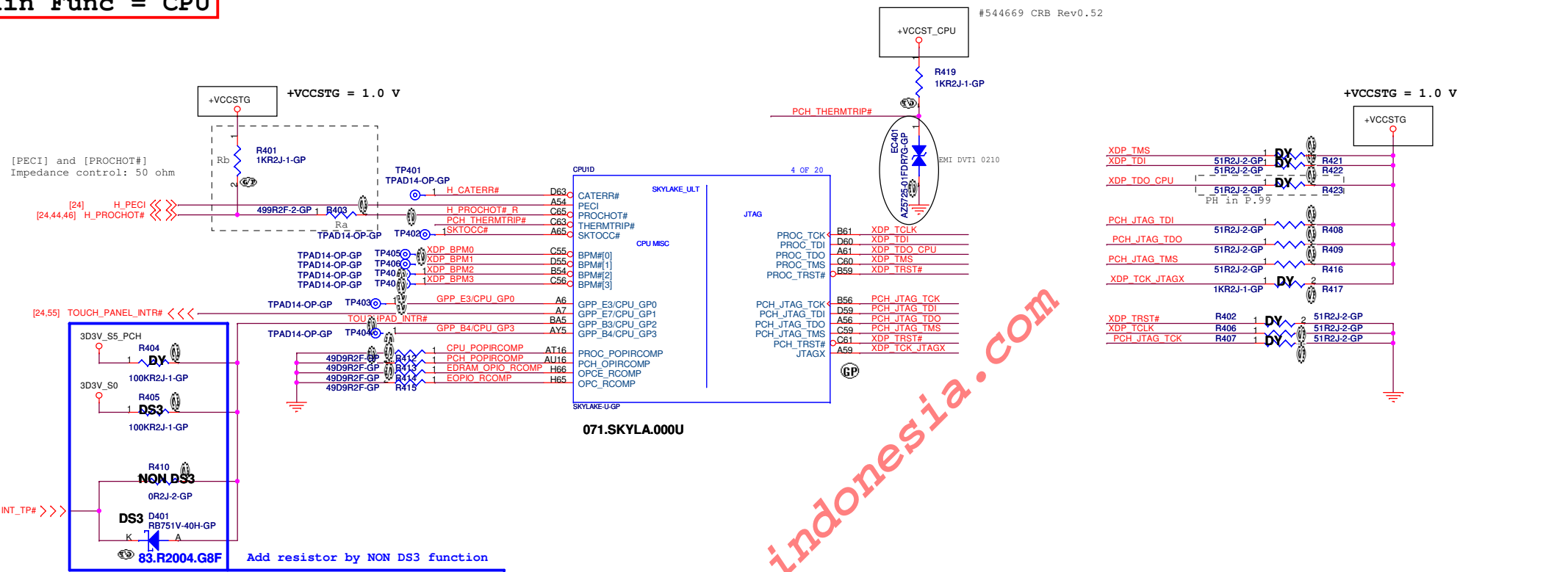
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Date: Thursday, February 18, 2016

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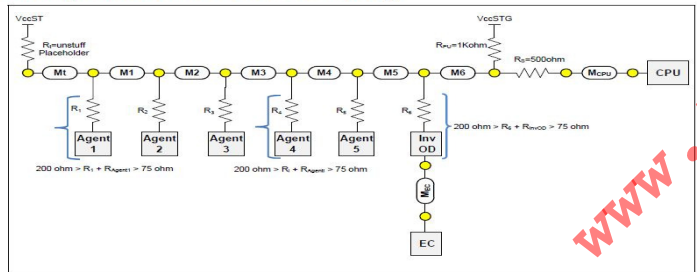
Main Func = CPU

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

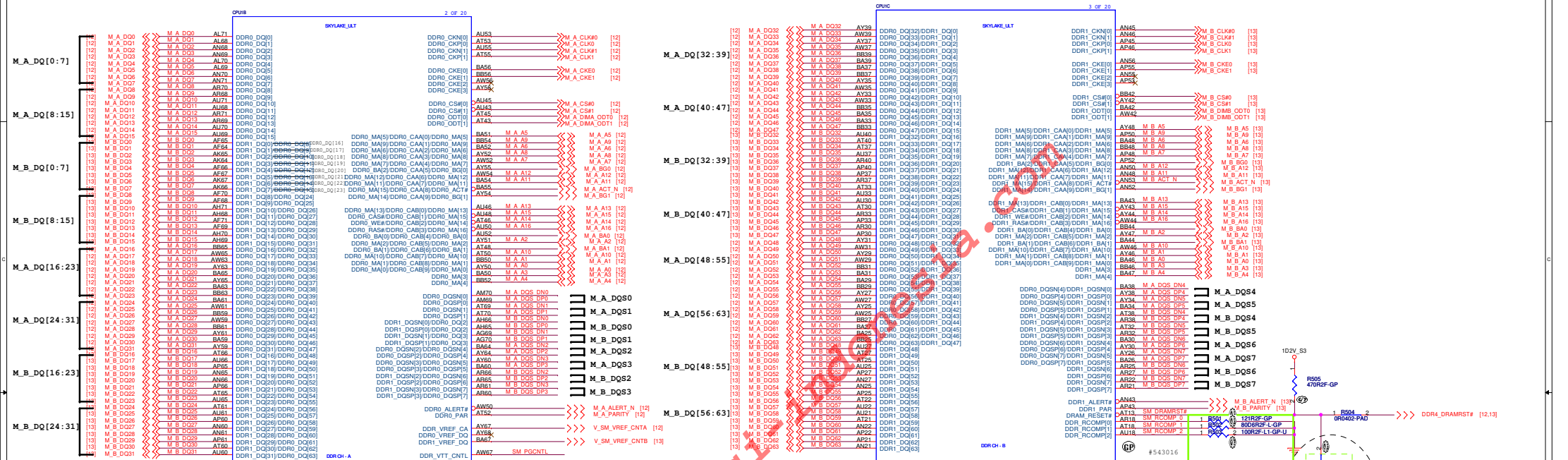


(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



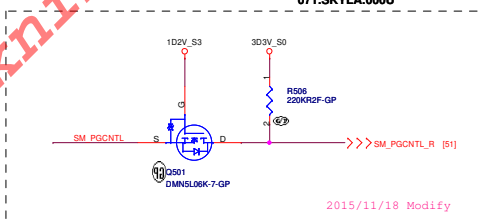
M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches



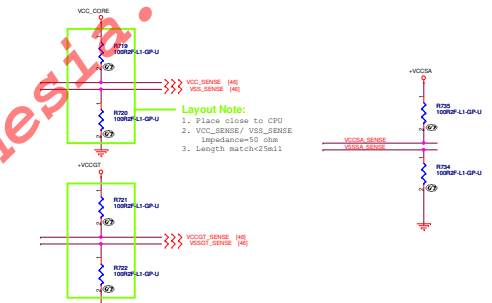
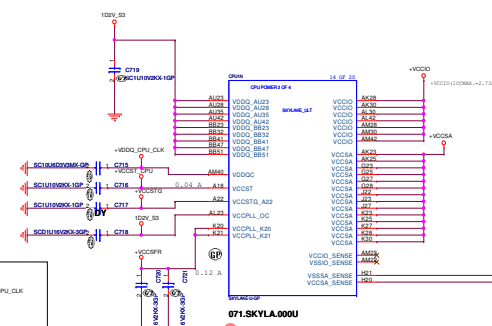
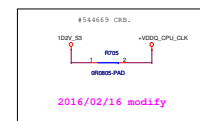
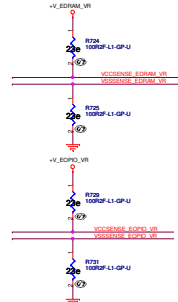
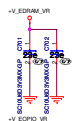
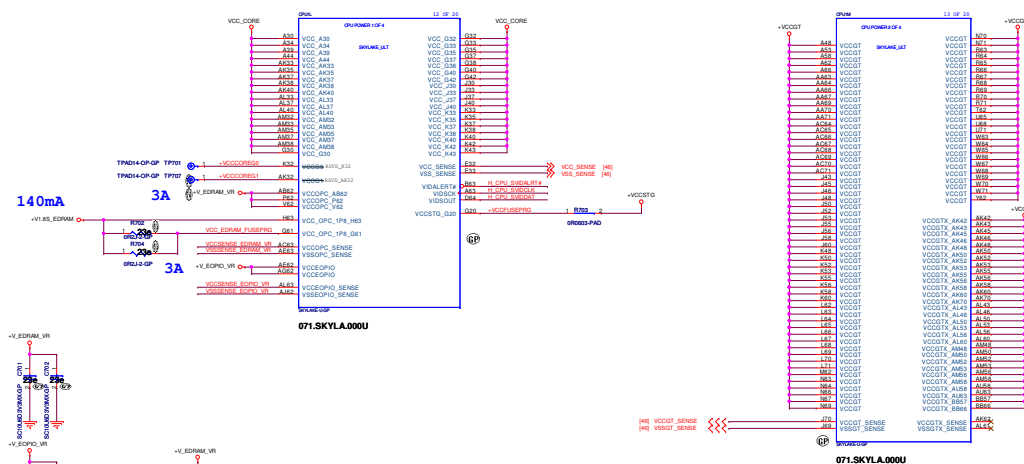
DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT 4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Processor	Memory Type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processors	DDR0_ODT[0] connected to DIMM Rank 0	Processor's ODT[0] connected to DIMM Rank 0	1, 2
SKL-U	LPDDR3 Memory Down	Processors	DDR0_ODT[0] connected to DIMM Rank 0	Processor's ODT[0] connected to DIMM Rank 0	1, 2
DDR3L Memory Down	Processors	Processors	DDR0_ODT[0] connected to DIMM Rank 0	Processor's ODT[0] connected to DIMM Rank 0	3, 4
DDR3L SO-DIMM	DIMM	Processors	DDR0_ODT[0] connected to DIMM Rank 0	Processor's ODT[0] connected to DIMM Rank 0	1, 3
DDR3L Head Memory Down	DIMM	Processors	DDR0_ODT[0] connected to DIMM Rank 0	Processor's ODT[0] connected to DIMM Rank 0	3, 4
DDR3L Head Memory SO-DIMM	DIMM	Processors	DDR0_ODT[0] connected to DIMM Rank 0	Processor's ODT[0] connected to DIMM Rank 0	1, 3
DDR4 Memory Down	Processors	Processors	DDR0_ODT[0] connected to DIMM Rank 0	Processor's ODT[0] connected to DIMM Rank 0	1, 3
DDR4 SO-DIMM	DIMM	Processors	DDR0_ODT[0] connected to DIMM Rank 0	Processor's ODT[0] connected to DIMM Rank 0	1, 3



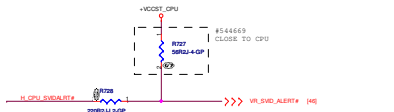
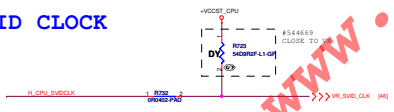
Design Guideline: SM-RCOMP keep routing length less than 500 mils. Layout Note: close to CPU



SVID DATA



SVID CLOCK



SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

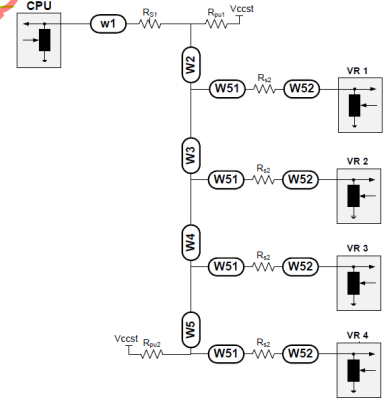
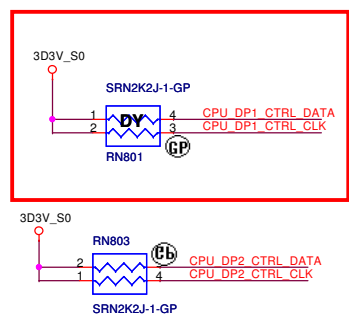


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W1 [inches]	W2 [inches]	R _{DS(on)} [Ω]	R _{DS(on)} [Ω]	R _{DS(on)} [Ω]	R _{DS(on)} [Ω]	V _{CE(sat)} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							56	45	0	50	
VIDALERT							y	220	0		

Dummy, Vendor suggest
20141117

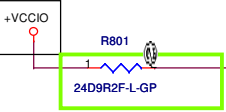


HDMI

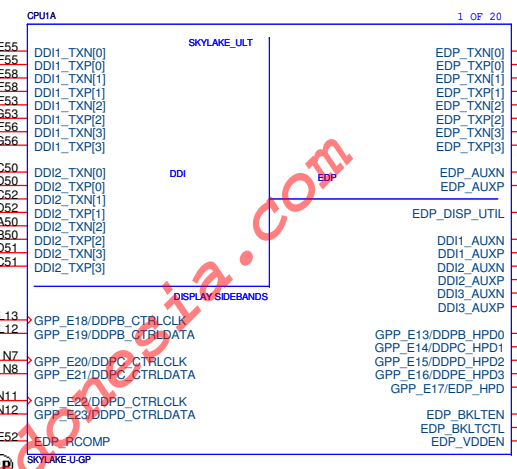
DP and DP to VGA

HDMI

Check



- [57] HDMI_DATA2#
- [57] HDMI_DATA2
- [57] HDMI_DATA1#
- [57] HDMI_DATA1
- [57] HDMI_DATA0#
- [57] HDMI_DATA0
- [57] HDMI_CLK#
- [57] HDMI_CLK
- [38] PCH_DPC_N0
- [38] PCH_DPC_P0
- [38] PCH_DPC_N1
- [38] PCH_DPC_P1
- [38] PCH_DPC_N2
- [38] PCH_DPC_P2
- [38] PCH_DPC_N3
- [38] PCH_DPC_P3



071.SKYLA.000U

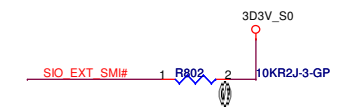
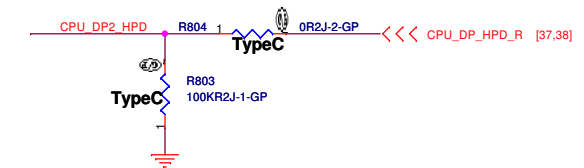
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC



Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 Ω \pm 1% resistor.

Main Func = CPU

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(#543016 PDS)

CORE

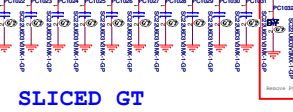
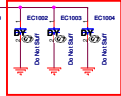
20140814 DAVID

U-line 23a 28W
IccMax current-10ms max = 34 A

220 0603 x 35 (5 DT)



SMT reserve , 20141118

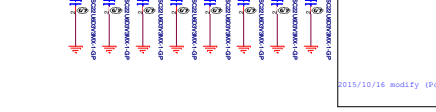
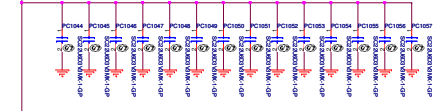
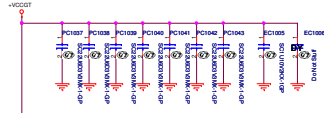


Remove PC1021 and EC1001 (power team request)

SLICED GT

U-line 23a 28W
IccMax current-10ms max[A] = 67 A

220 0603 x35 (5 DT)



2015/10/16 modify (Power team request)

VCCSA

220 0603 x13 (5 DT)

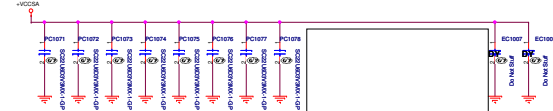


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (04.5mD ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (04.5mD ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (04.5mD ESR)	Placed at primary side near to VR output
VCCGTx Power Plane at VR output	1x 220uF (04.5mD ESR)	Placed at primary side near to VR output
VCCIO Power Plane at VR output	2x 47uF 0805	Additional components needed when supporting 23a
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

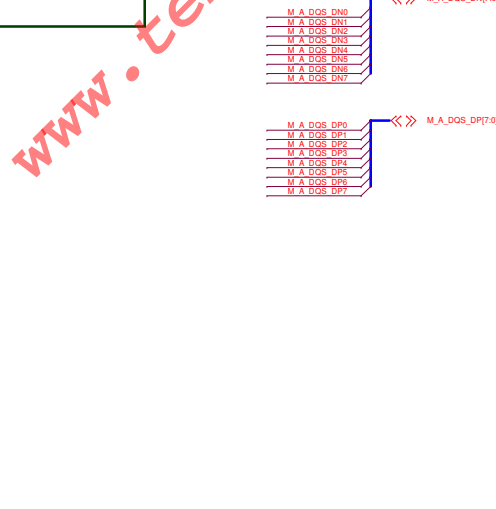
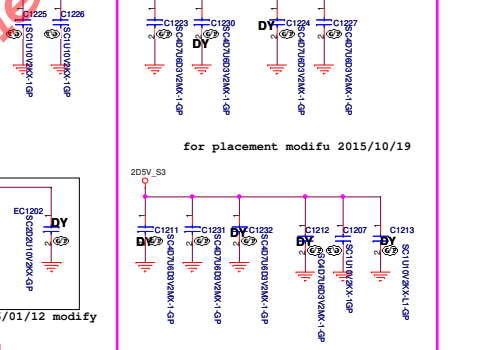
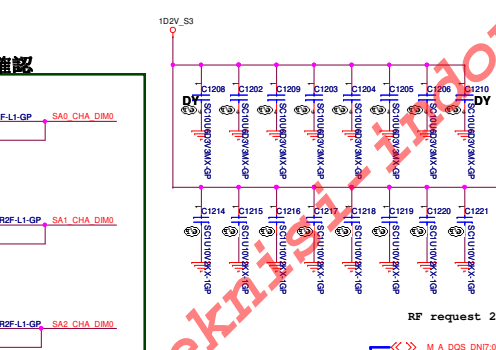
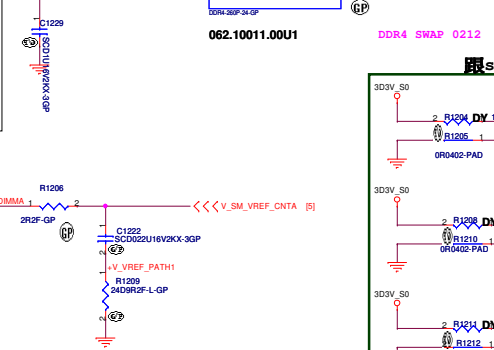
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

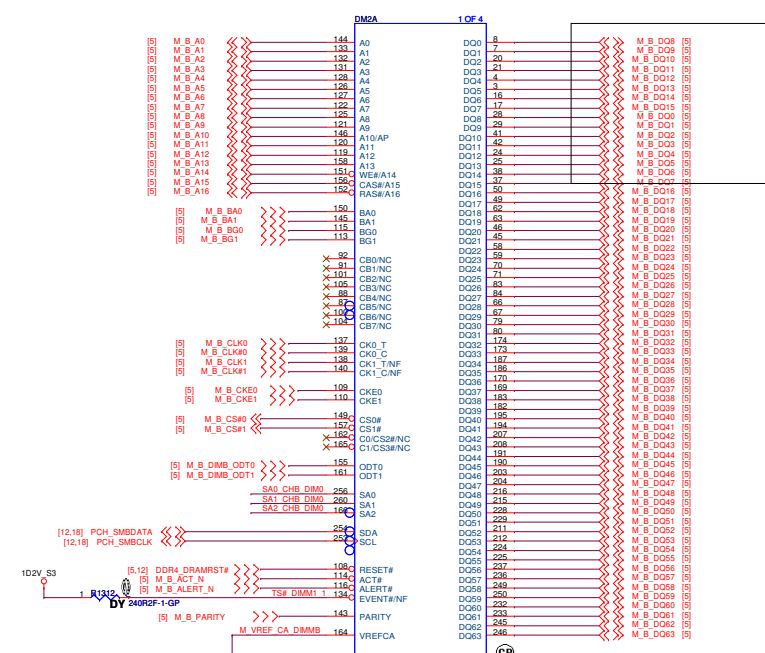
Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 220uF 0805		Place on secondary side, underneath the package
VCC	7x 10uF 0402		
VCC	15x 1uF 0201		
VCC		8x 47uF 0805 (6.3V)	Place as close to the package as possible
VCC		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
VCCGT		12x 1uF 0201	
VCCGT		3x 47uF 0805 (6.3V)	Place as close to the package as possible
VCCGT		7x 22uF 0603	
VCCGT		3x 47uF 0805	Place as close to the package as possible
VCCGT		5x 22uF 0603	Additional components needed when supporting 23a
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package
VCCGTx		8x 22uF 0603	Only needed when supporting 23a
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
VCCSA		7x 1uF 0201	
VCCSA		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCIO		4x 1uF 0201	
VDDQ	2x 10uF 0402		Place as close to the package as possible
VDDQ		4x 1uF 0201	
VDDQ		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCSTG			Placeholder only
VCCSTG	2x 10uF 0402		Place on secondary side, underneath the package
VCCSTG			Place on secondary side, underneath the package
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCSTG			Place as close to the package as possible

Title			
CPU (Power CAP2)			
Size A3	Document Number		Rev
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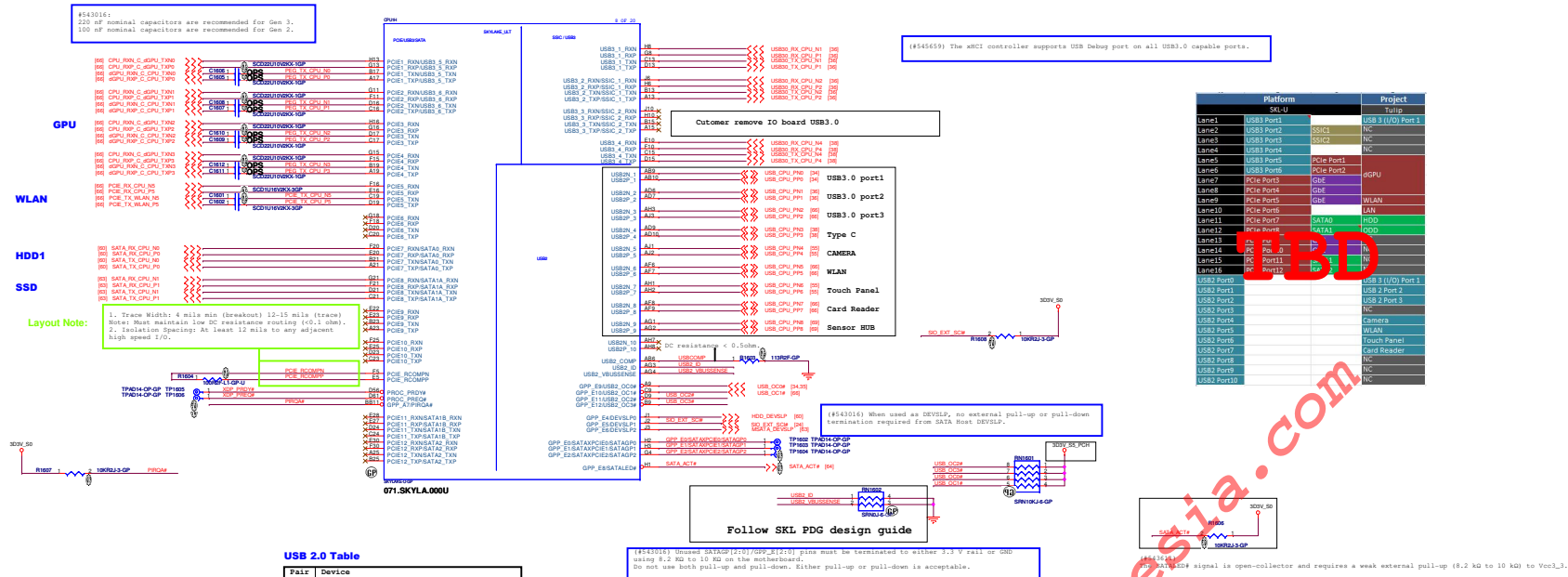


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Title (Reserved)_SODIMM _SODIMM4					
Size A4		Document Number Starload SKL-U			Rev A00
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Platform	SKL-U	Project
Lane1	USB3 Port1	Tulip
Lane2	USB3 Port2	SSIC
Lane3	USB3 Port3	SSIC
Lane4	USB3 Port4	NC
Lane5	USB3 Port5	PCie Port2
Lane6	USB3 Port6	PCie Port2
Lane7	PCie Port3	GbE
Lane8	USB3 Port5	GbE
Lane9	PCie Port5	GbE
Lane10	PCie Port6	LAN
Lane11	PCie Port7	SATA
Lane12	PCie Port8	SATA
Lane13	PCie Port9	IN
Lane14	PCie Port10	IN
Lane15	PCie Port11	IN
Lane16	PCie Port12	IN
USB2 Port0		USB 3 (U/D) Port 1
USB2 Port1		USB 3 Port 2
USB2 Port2		USB 3 Port 3
USB2 Port3		NC
USB2 Port4		Camera
USB2 Port5		WLAN
USB2 Port6		WLAN
USB2 Port7		Touch Panel
USB2 Port8		Card Reader
USB2 Port9		NC
USB2 Port10		NC

USB 2.0 Table

Port	Device
0	USB3.0 port1
1	USB3.0 Port2 (Debug Port/IOBD)
2	USB3.0 Port3 (IOBD)
3	Sensor HUB
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

Table 24-2. PCI Express* Port Feature Details

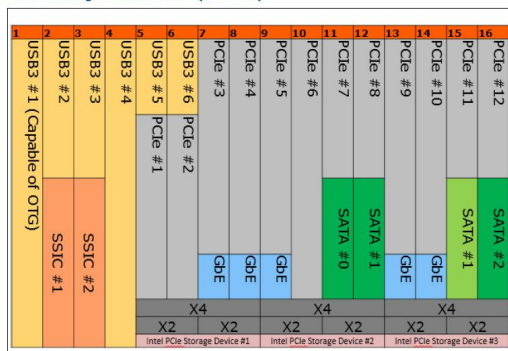
SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (M/s)	Theoretical Max Bandwidth (GB/s)		
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

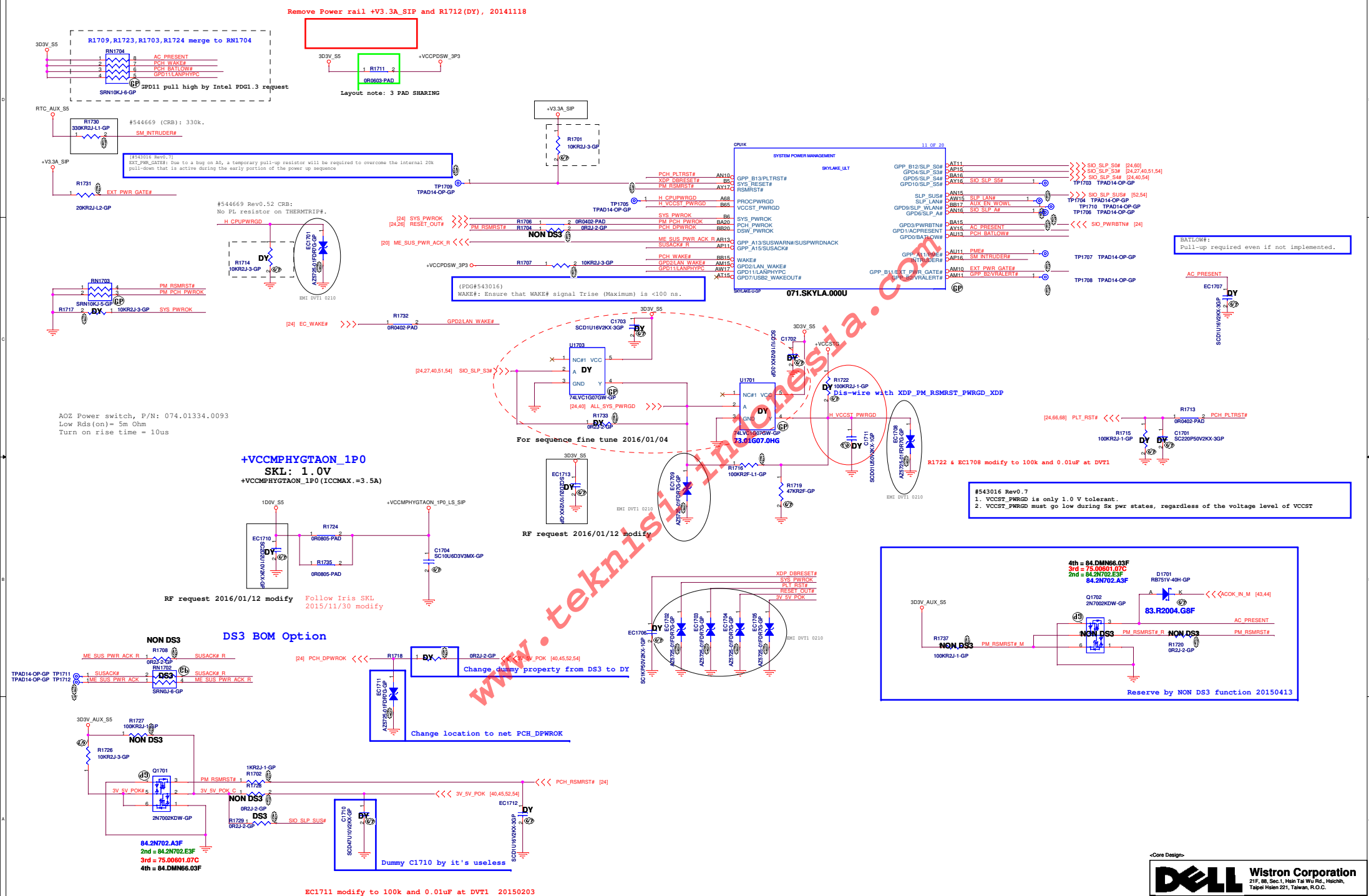
Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
U	1x4	Port1	Port3	Port5	Port7	Port9	Port11	Port12					
	2x2	Port1	Port3	Port5	Port7	Port9	Port11	Port12					
	1x2 + 2x1	Port1	Port3	Port4	Port5	Port7	Port8	Port9	Port10	Port11	Port12		
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x4	Port1	Port3	Port5	Port7	Port9	Port11	Port12					
	2x2	Port1	Port3	Port5	Port7	Port9	Port11	Port12					
	1x2 + 2x1	Port1	Port3	Port4	Port5	Port7	Port8	Port9	Port10	Port11	Port12		
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9	Port10		
	2x1									Port9	Port10		

#545659 (SKL_PCH_U_XD0 Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

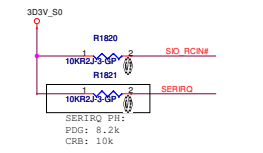
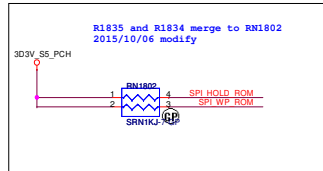




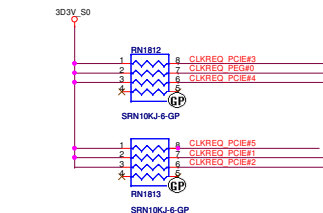
PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

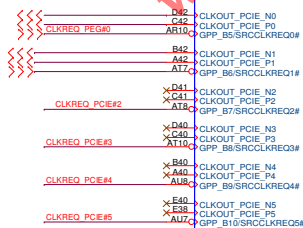
This signal has a weak internal pull-down.



RCIN#:
Frequency to Avoid: 33 MHz



WLAN



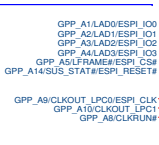
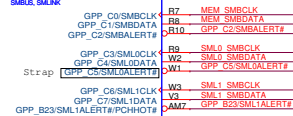
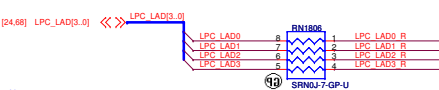
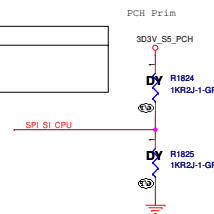
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PCH strap pin:

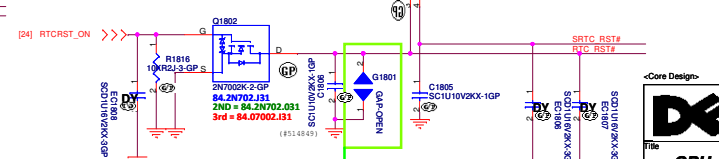
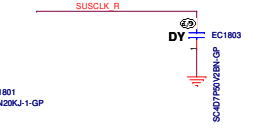
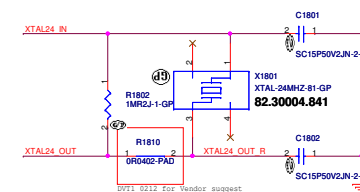
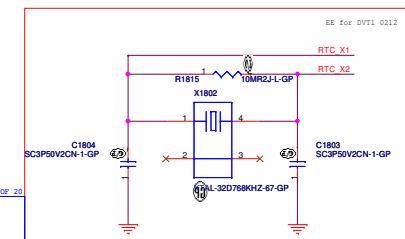
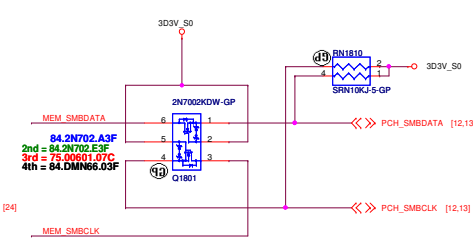
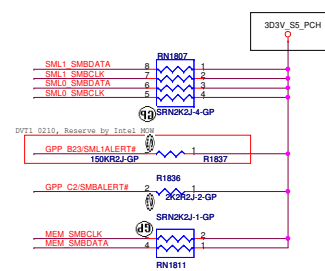
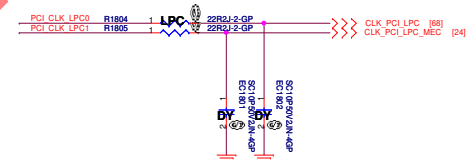
BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

This signal has a weak internal pull-up



20140820 DAIVD



Layout: Place at the open door area.

«Core Design:



Title

CPU (LPC/SPI/SMBUS/CL/CLK)		
Size	Document Number	Rev

A2	Starload SKL-U	A00
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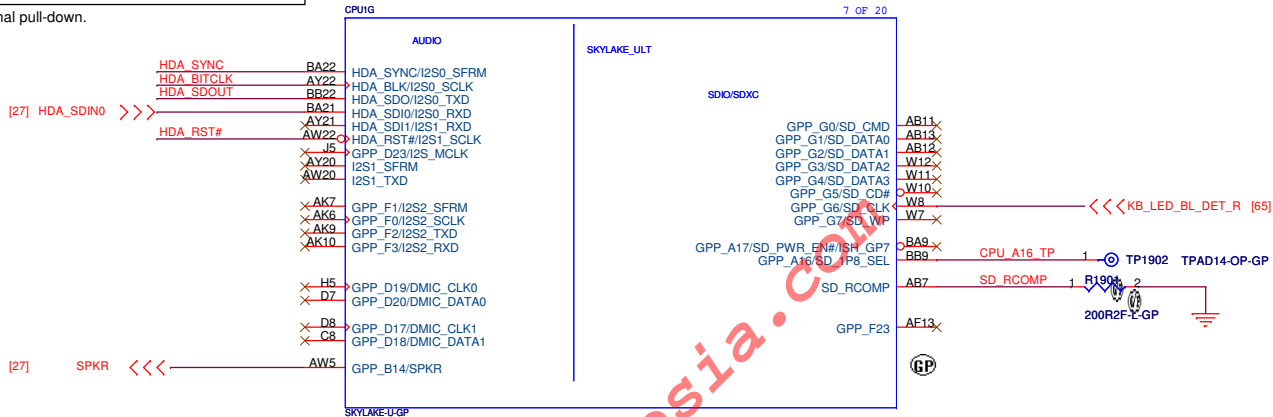
Date: Thursday, February 25, 2016 Sheet 18 of 106

Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

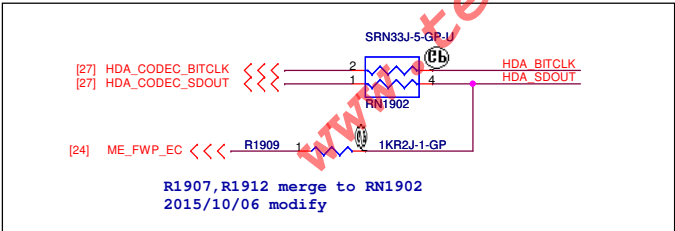
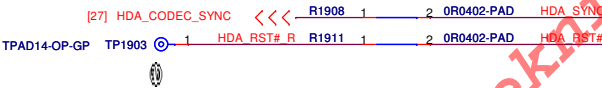
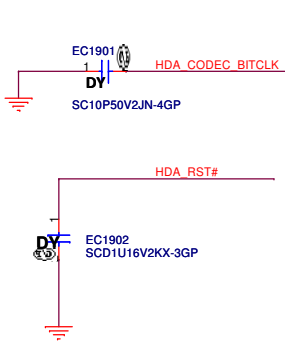
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

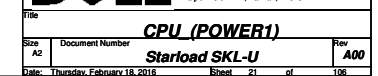


<Core Design>

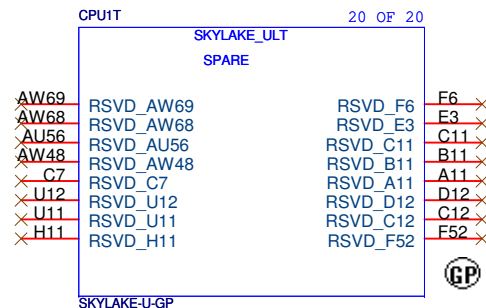


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Title CPU (AUDIO/SDIO/SDXC)		
Size A3	Document Number Starload SKL-U	Rev A00
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Main Func = PCH



071.SKYLA.000U

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Title

CPU (RSVD)

Size
A4

Document Number

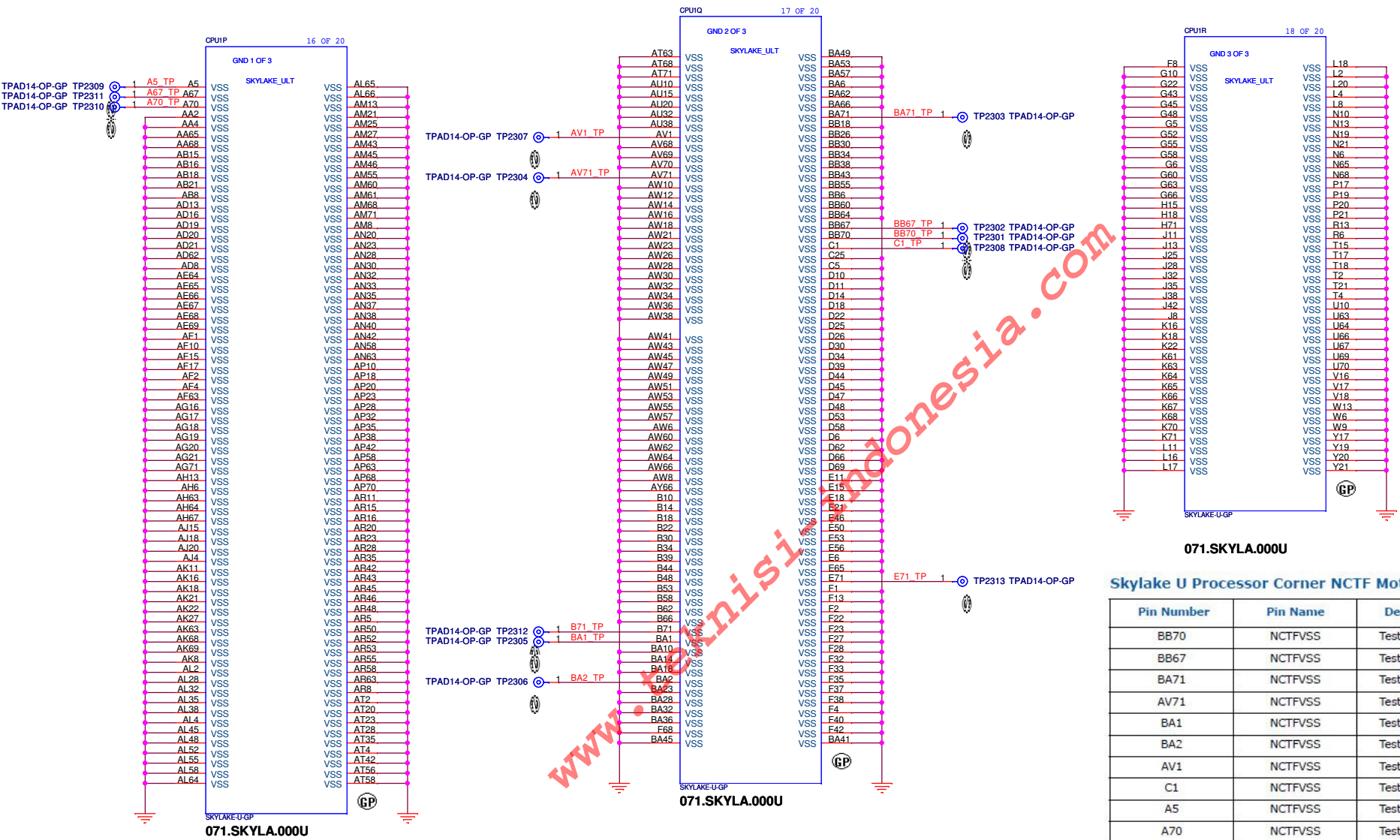
Starload SKL-U

Rev
A00

Date: Thursday, February 18, 2016

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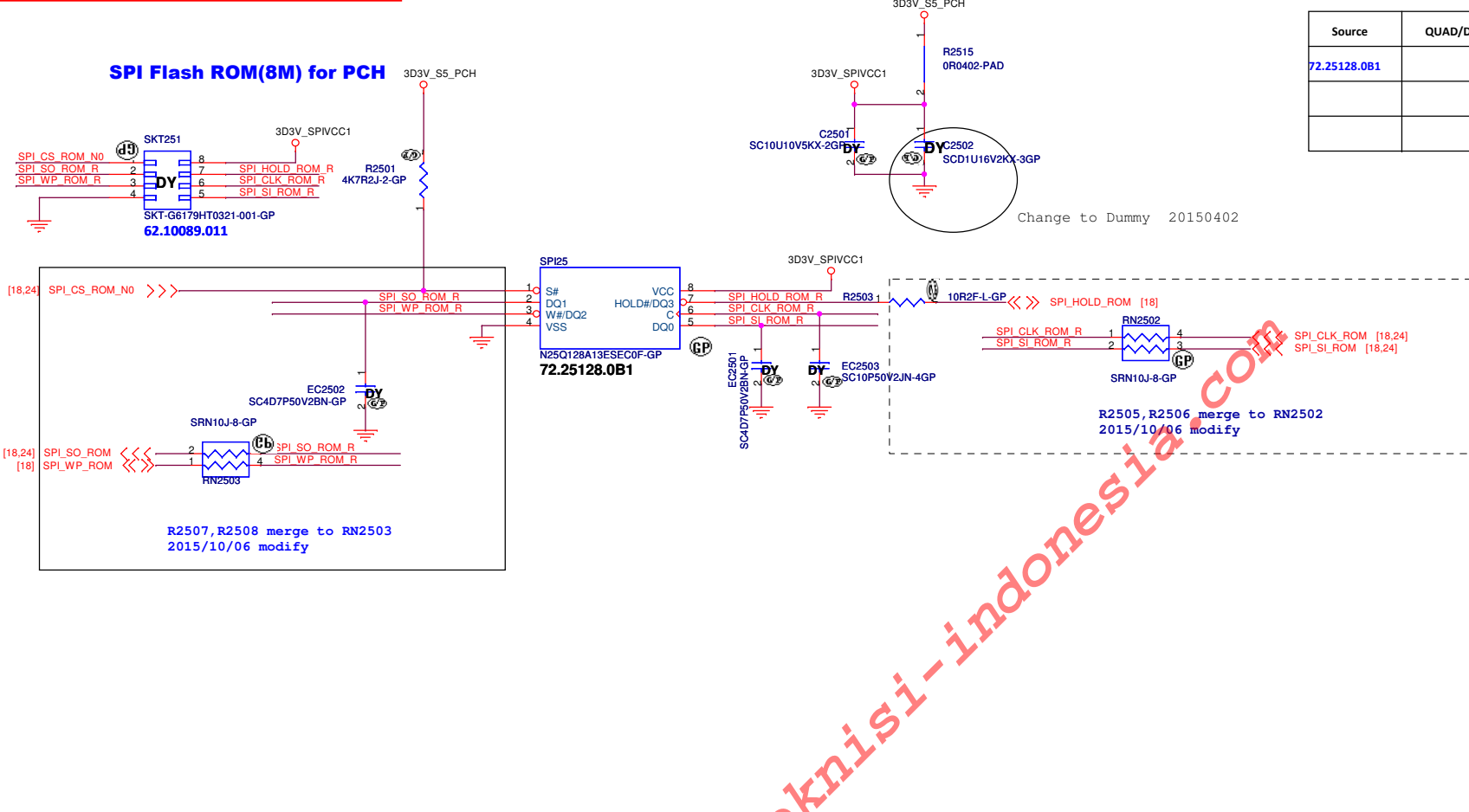
Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

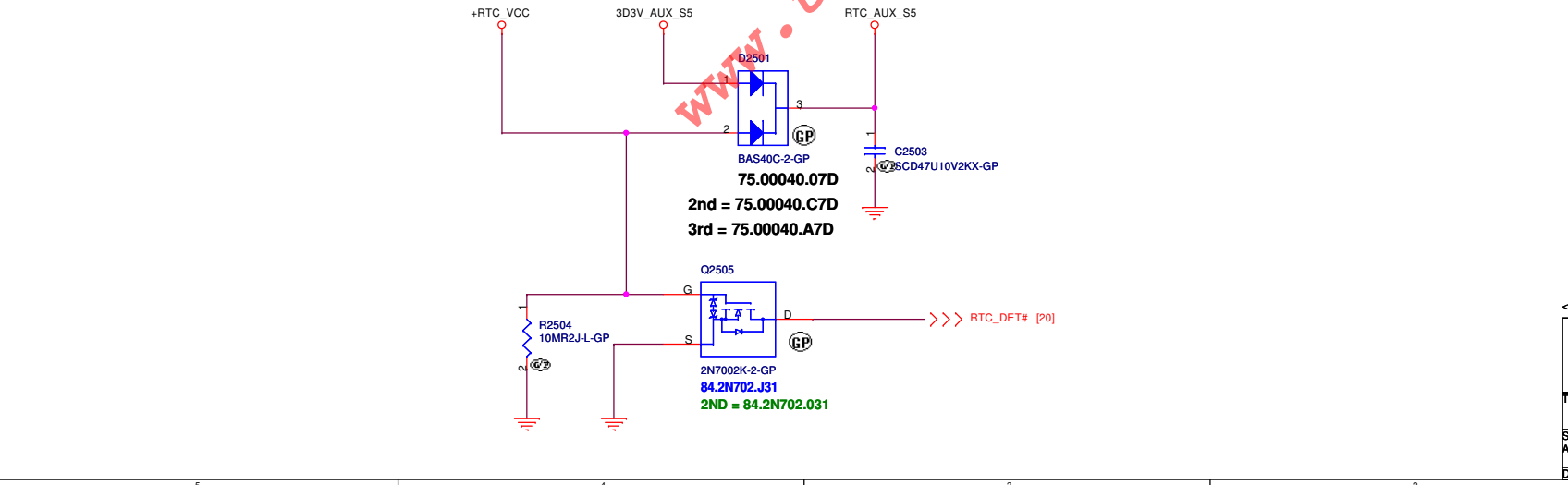
Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

Main Func = SPI Flash




Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25128.0B1	O	O	O
	O	O	O
	O	O	O

Main Func = RTC



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TitleFlash/RTC

SizeA3

Document NumberStarload SKL-U

RevA00

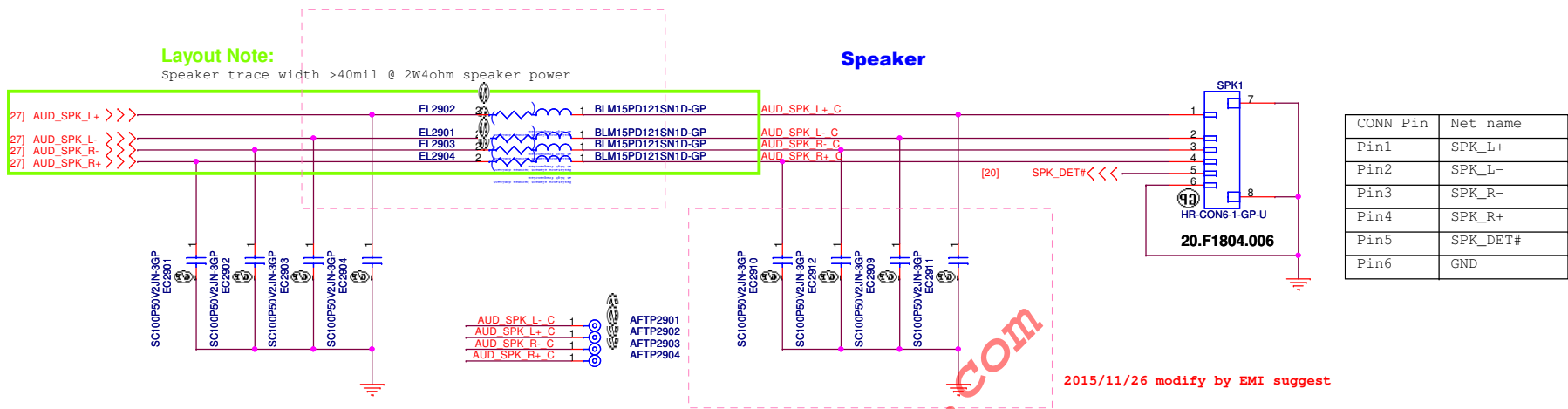
DateThursday, February 25, 2016

Sheet25 of 106

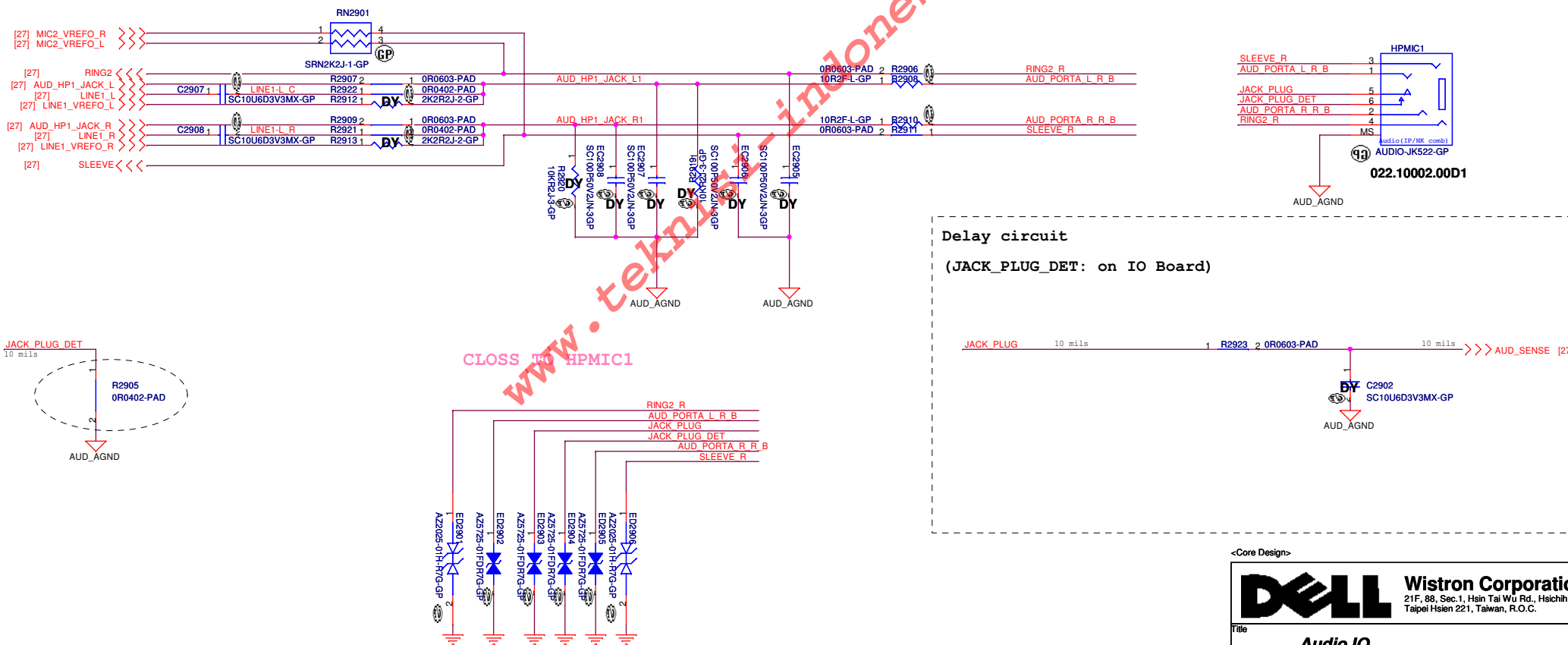


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Main Func = Audio



Universal Jack (Moved to I/O Board)



Main Func = Audio

(Blanking)

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Title (Reserved)			
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Main Func = LAN

(Blanking)

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Title

XFOM&RJ45

Size
A3

Document Number
Starload SKL-U

Rev
A00

Date: Thursday, February 18, 2016

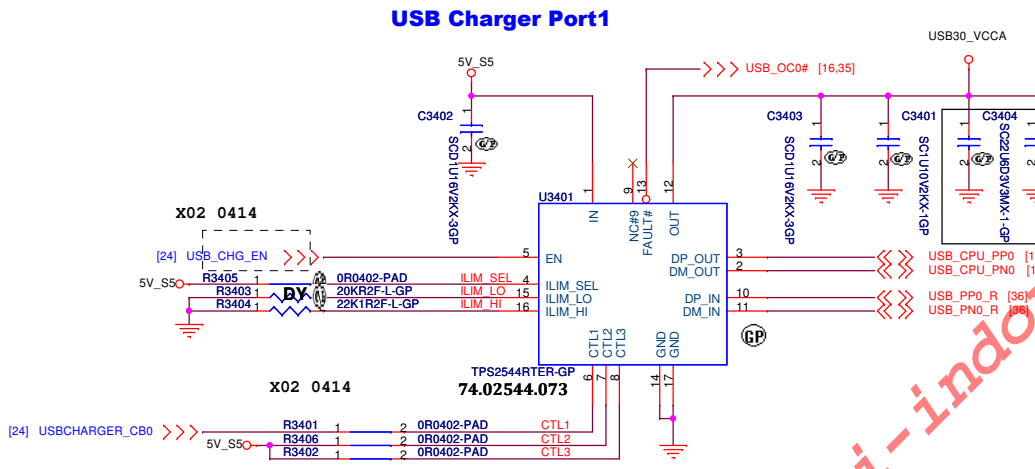
Sheet 32 of 106

1

5
Main Func = Card Reader

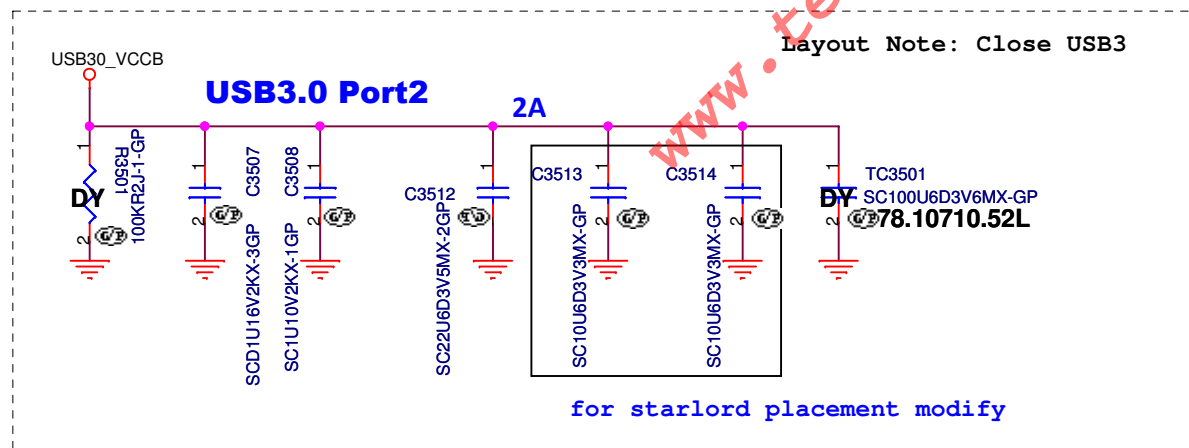
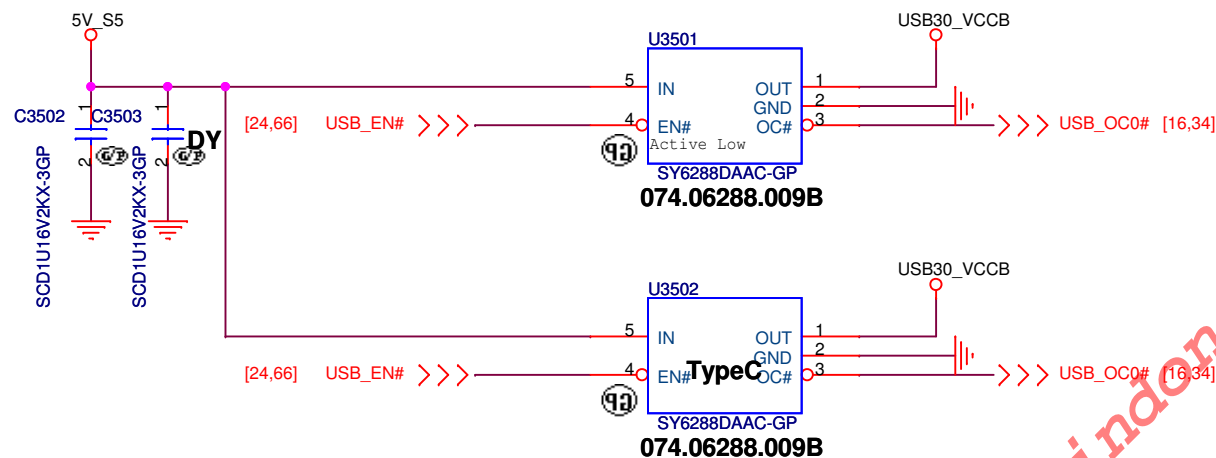
(Blanking)

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Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

Main Func = USB3.0 Port1



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Title

USB switch

Size

Document Number

Starload SKL-U

Rev

A00

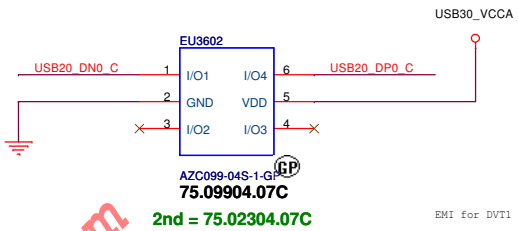
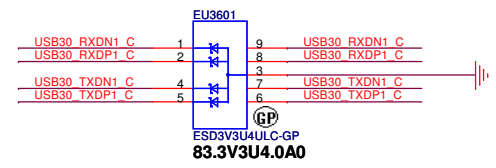
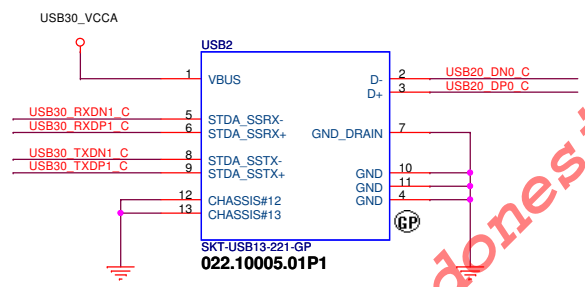
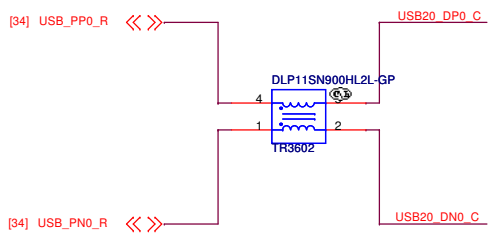
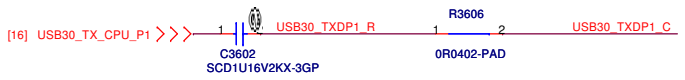
Date: Thursday, February 25, 2016

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Main Func = USB3.0 Port1

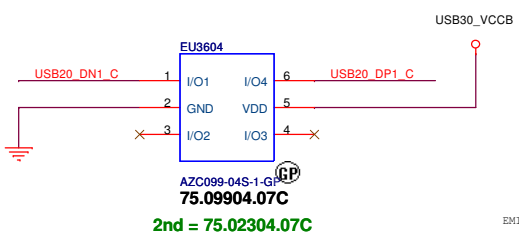
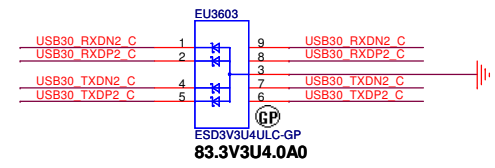
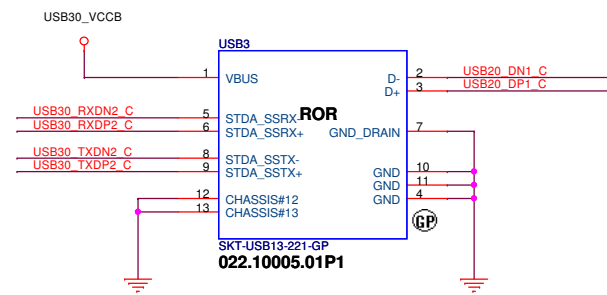
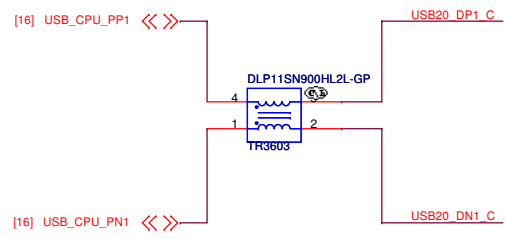
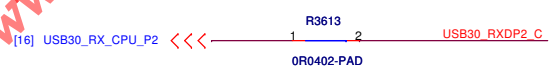
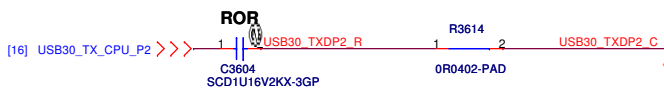
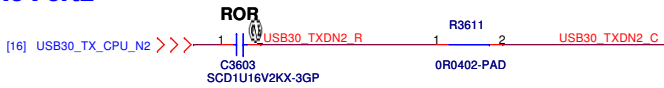
USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB3.0 Port2



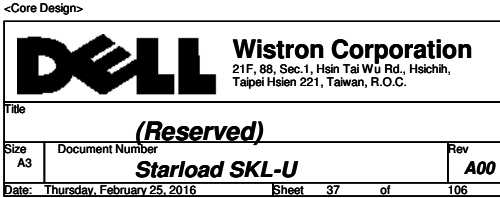
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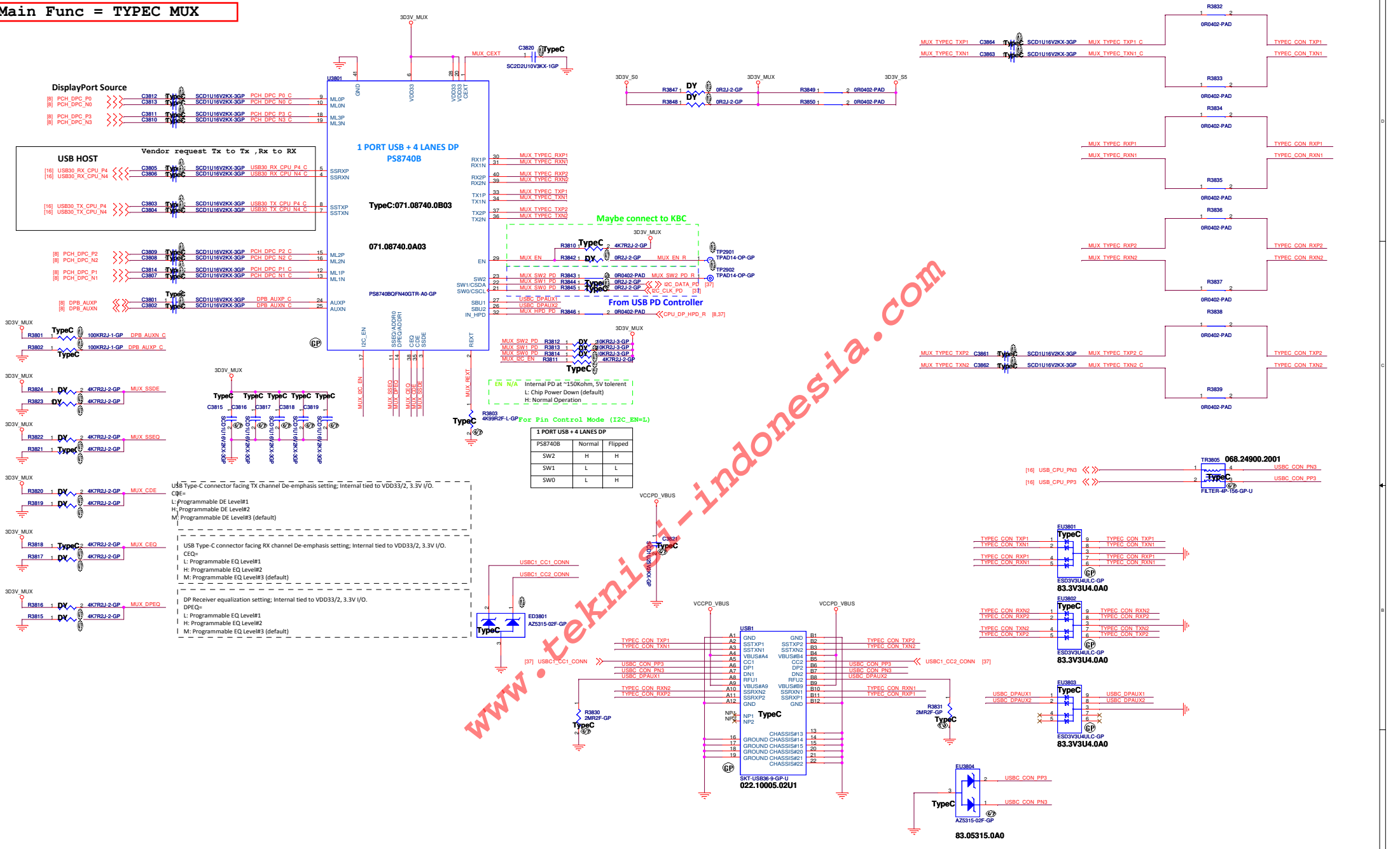
Title: **USB30**

Size: A3 Document Number: **Starload SKL-U** Rev: **A00**

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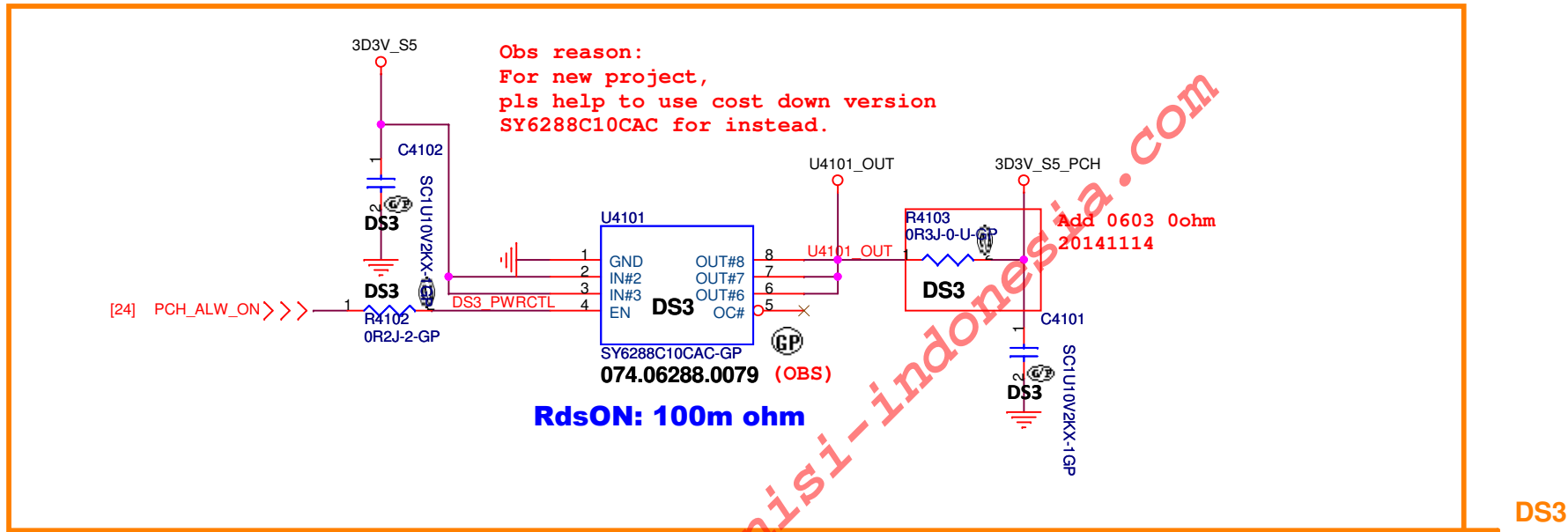


Main Func = TYPEC MUX



1 PORT USB + 4 LANES DP		
PS7408	Normal	Flipped
SW2	H	H
SW1	L	L
SW0	L	H

Main Func = Power Plane & Sequence



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Title
Connected_Standby(1/2)+DS3

Size A4	Document Number Starload SKL-U	Rev A00
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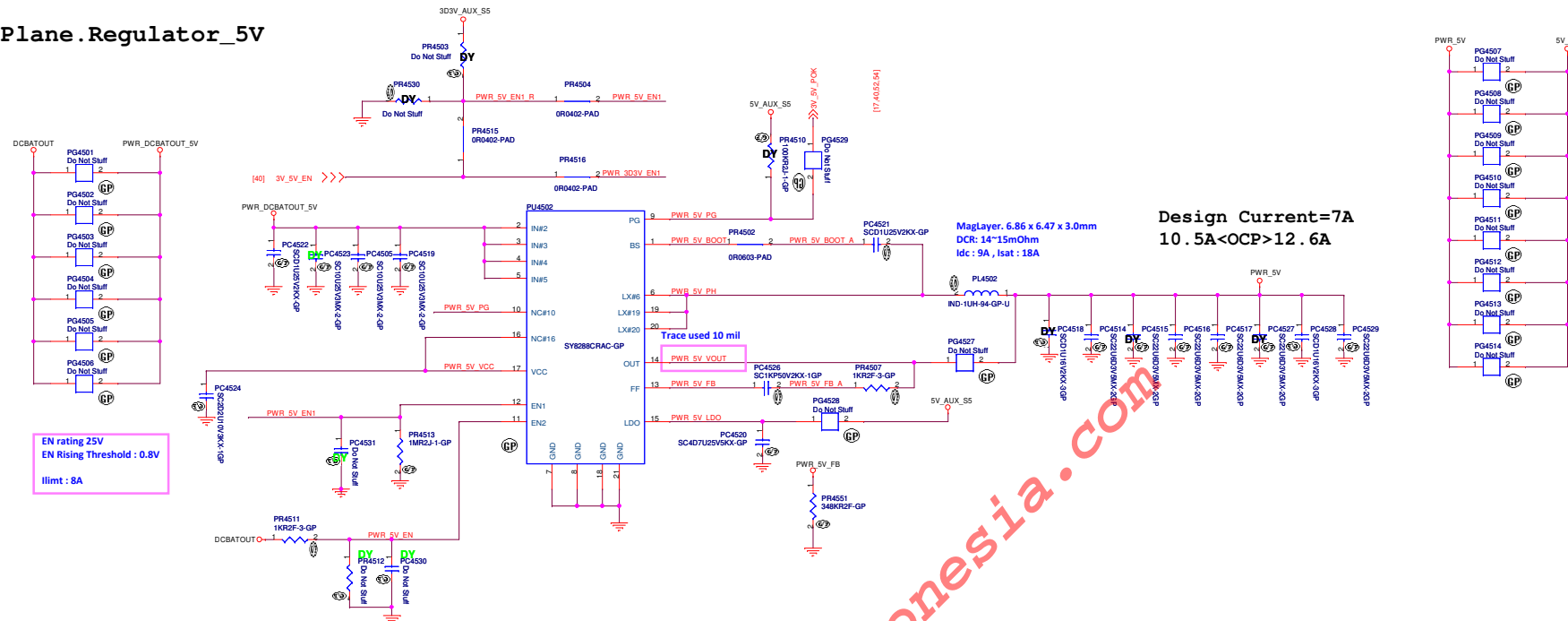
Main Func = DIMM1
Main Func = DIMM2

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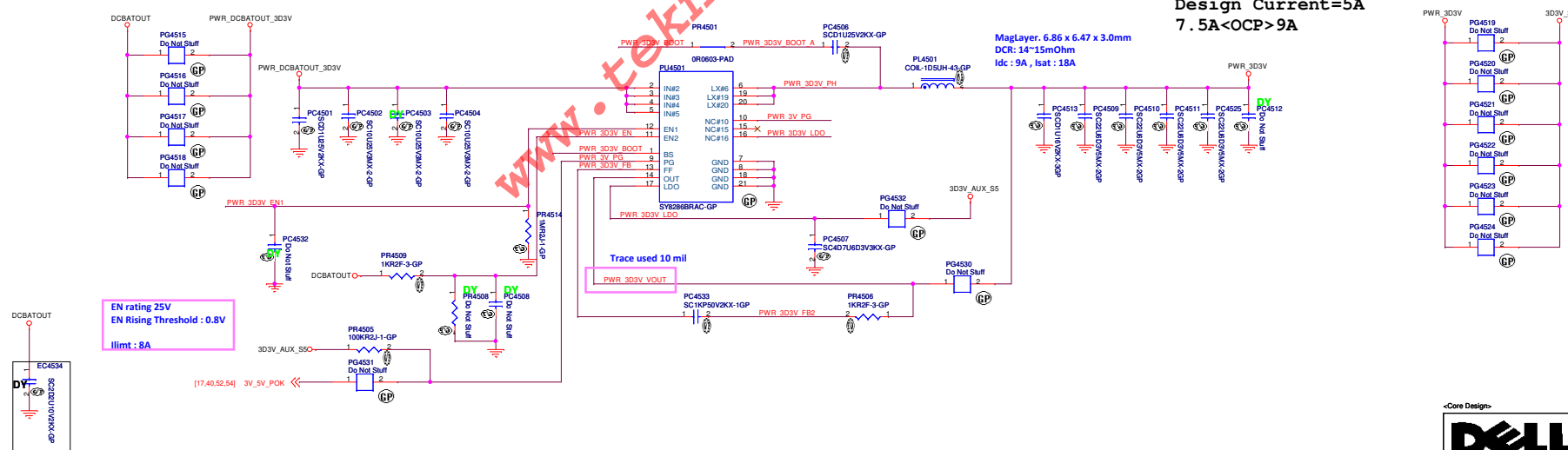


PR4433	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k

```
SSID = PWR.Plane.Regulator_5V
```

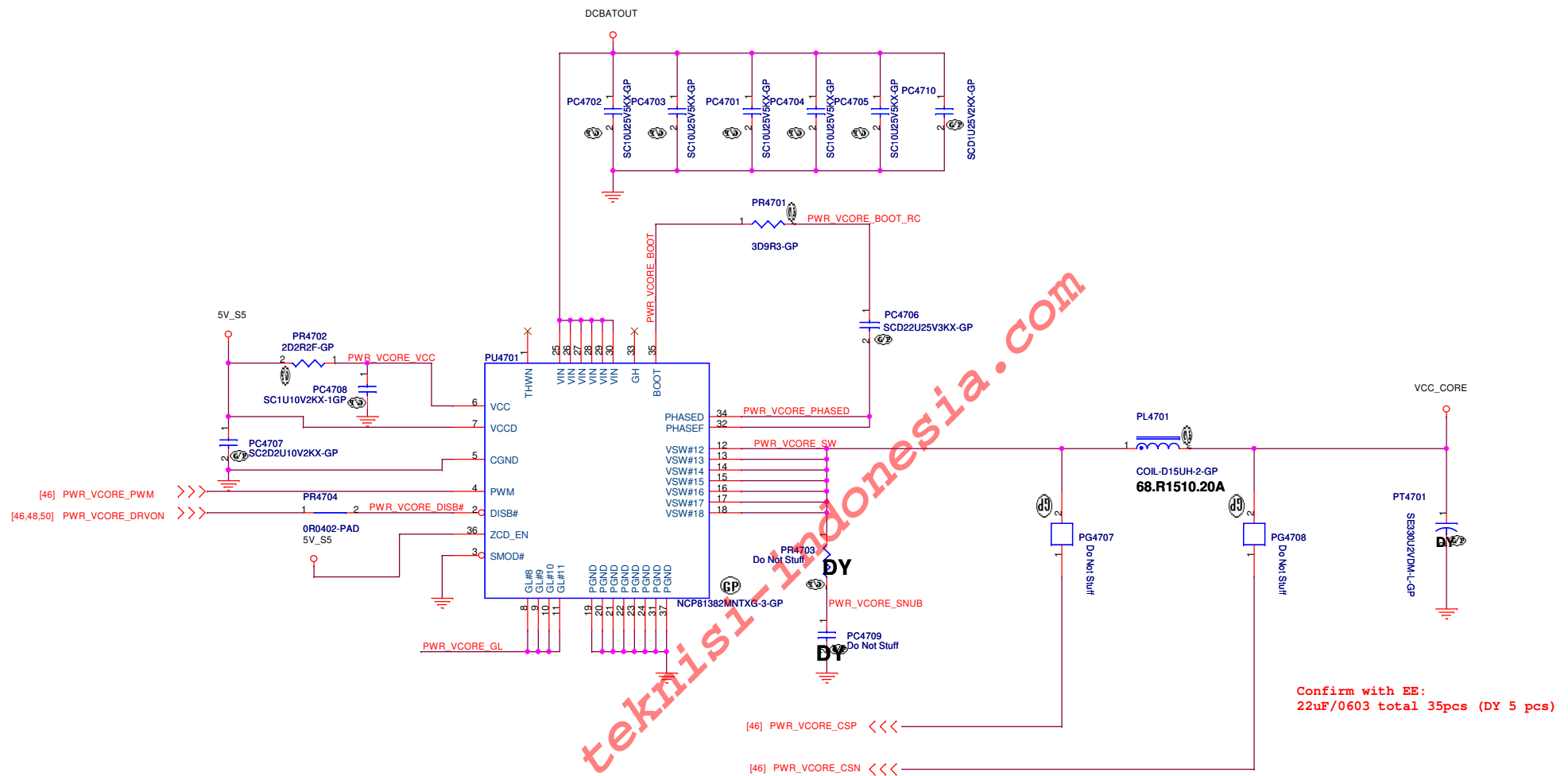


```
SSID = PWR.Plane.Regulator_3D3V
```



RF request 2016/01/12 modify


```
Main Func = CPU_CORE
```



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Title	Author	Year	Journal	Volume	Page
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NCP81382MN_CPU_VCORE(2/3)

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A3

Document Number

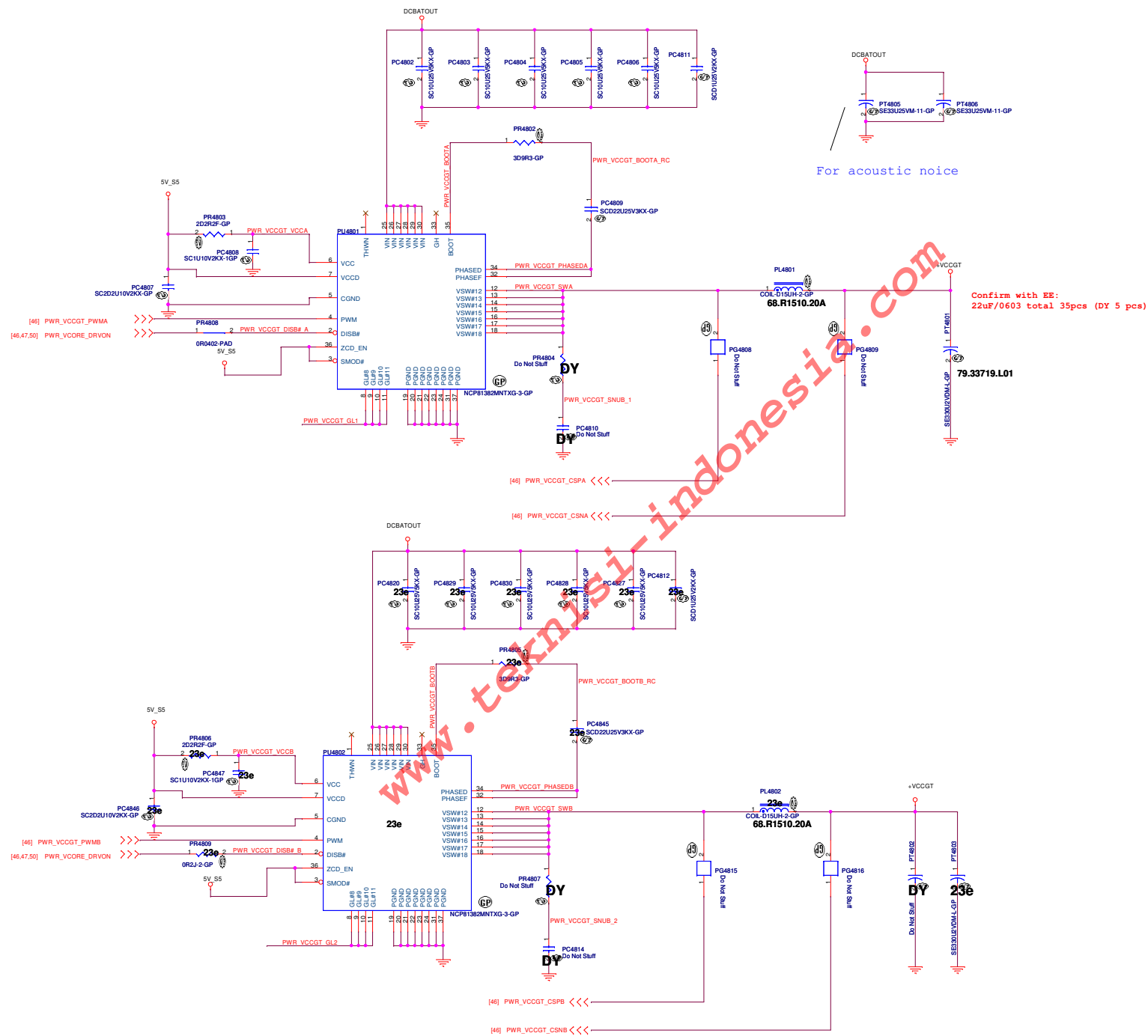
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Starload SKL-U

Rev
A00

Date: Thursday, February 25, 2016

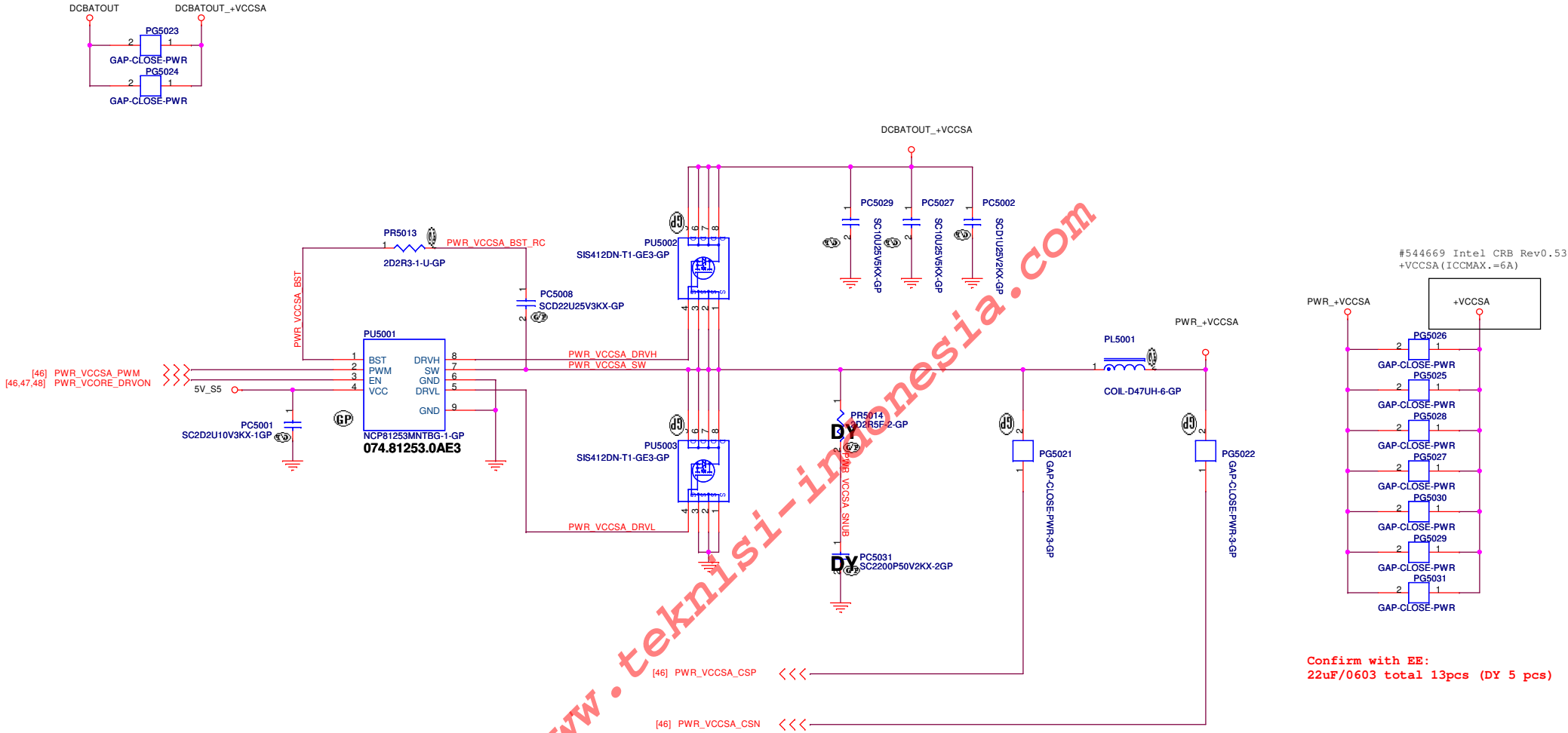
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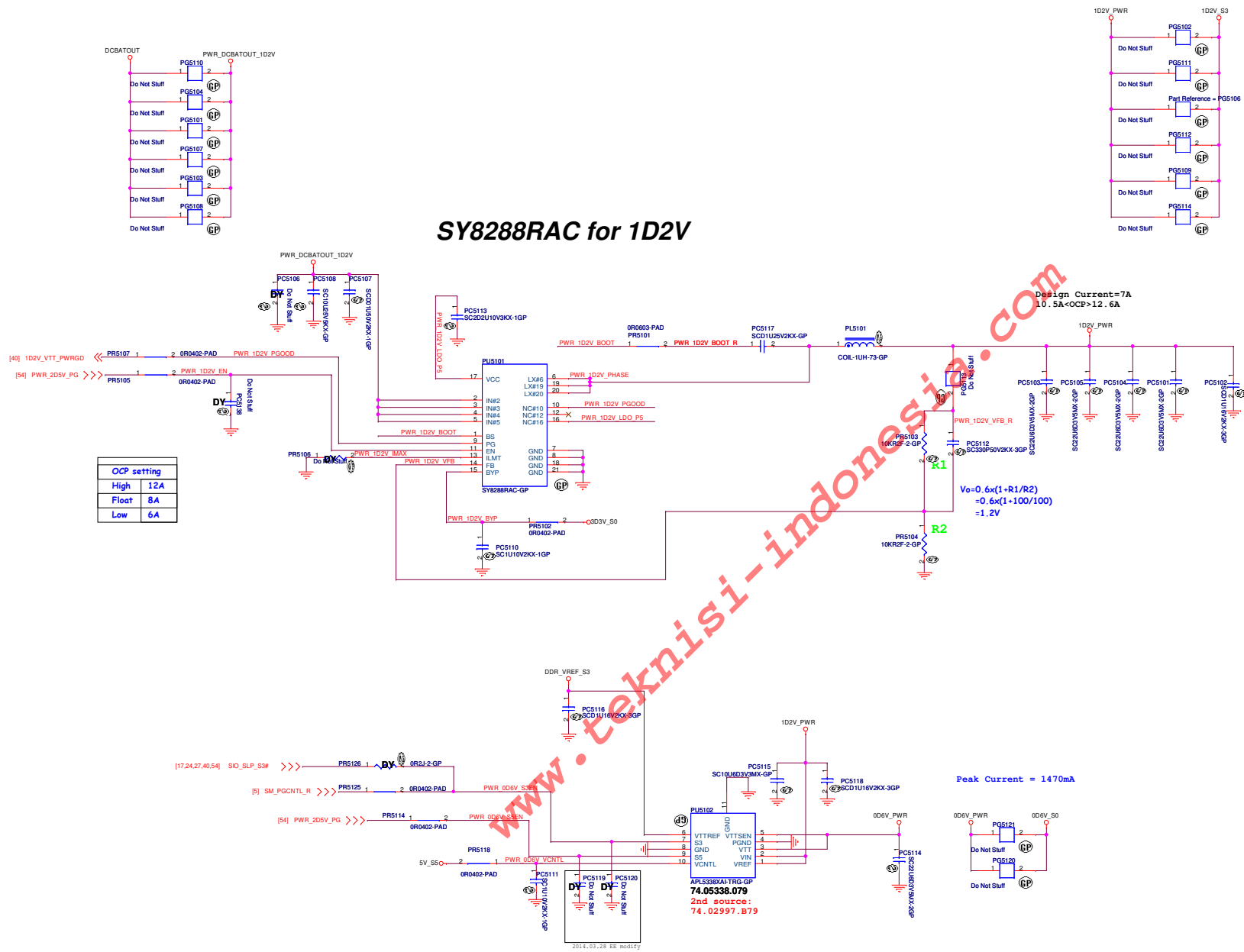
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Main Func = CPU_CORE
```



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Main Func = CPU_CORE

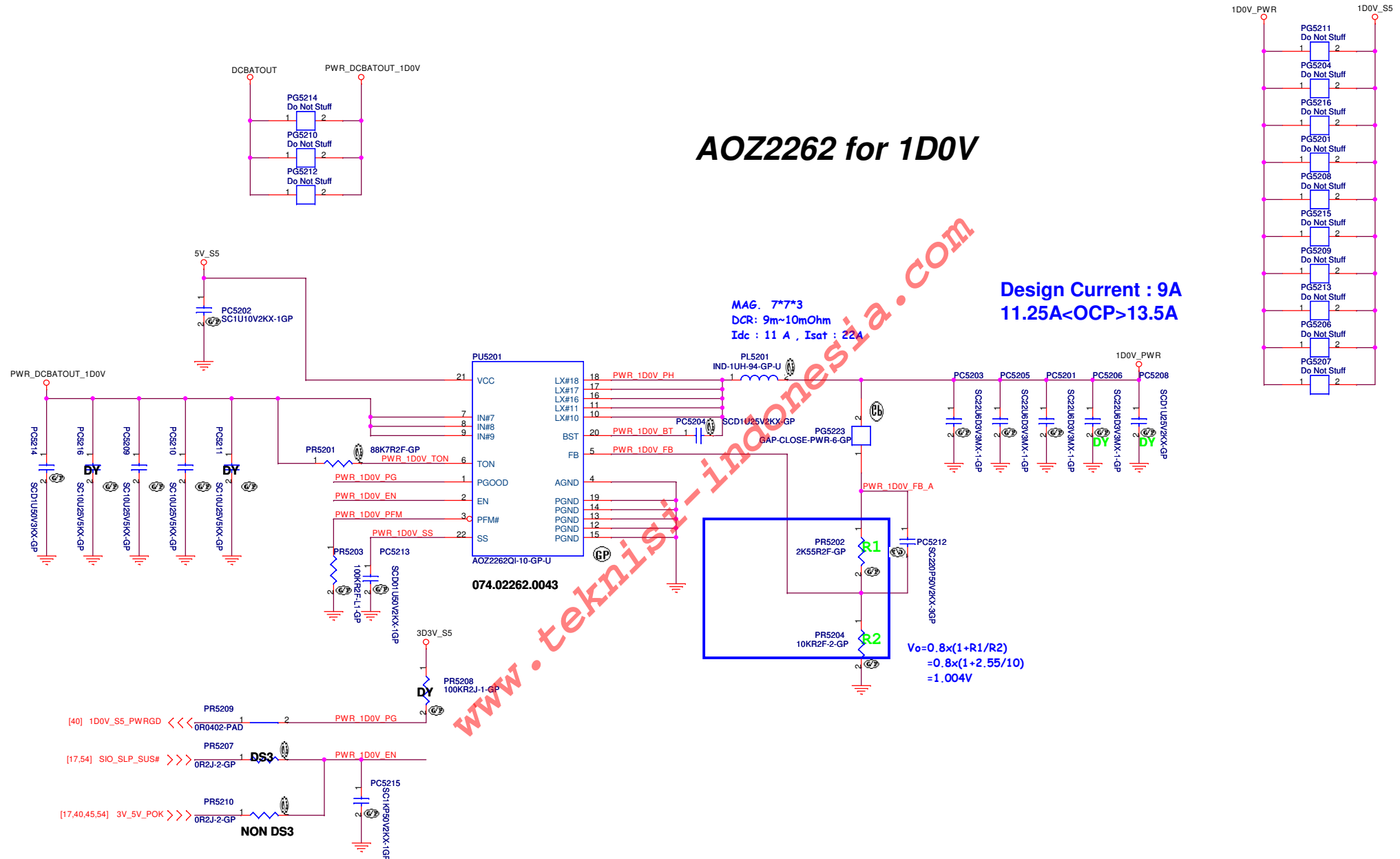




SSID = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D0V


Design Current : 9A
11.25A<OCP>13.5A



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Title

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Size

A3

Document Number

Starload SKL-U

Rev

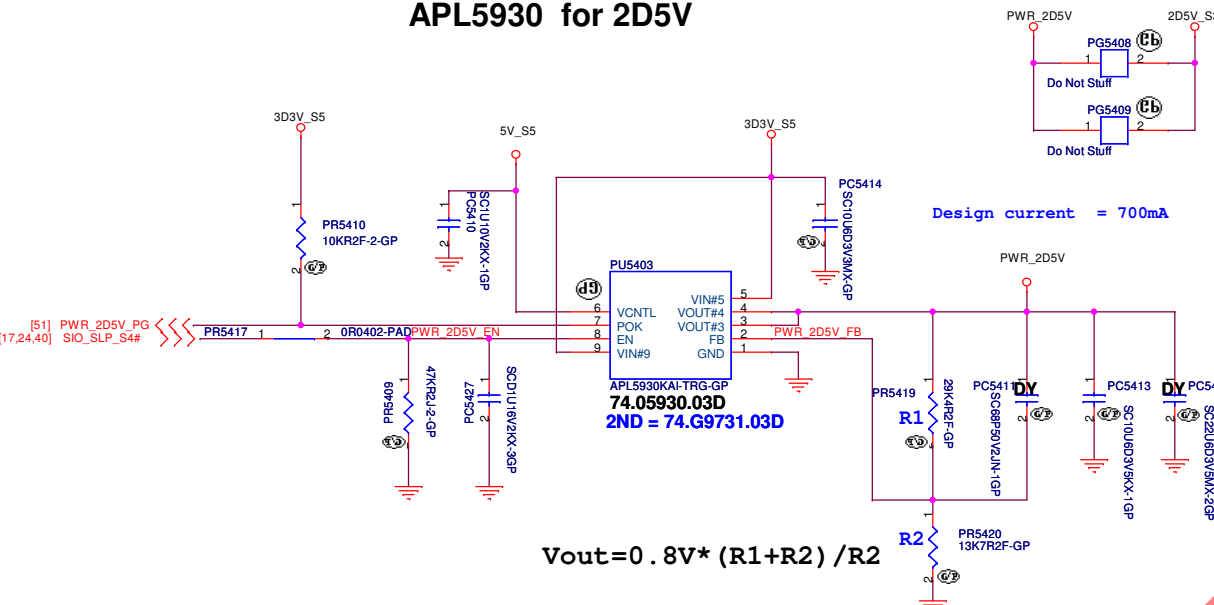
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Date: Thursday, February 18, 2016

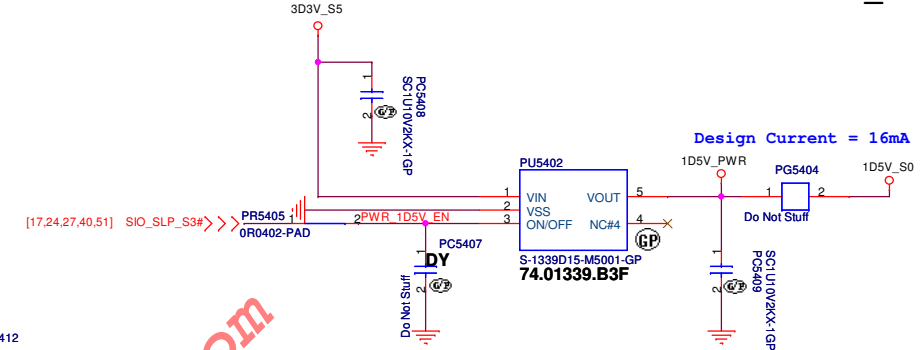
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Main Func = 1D5V

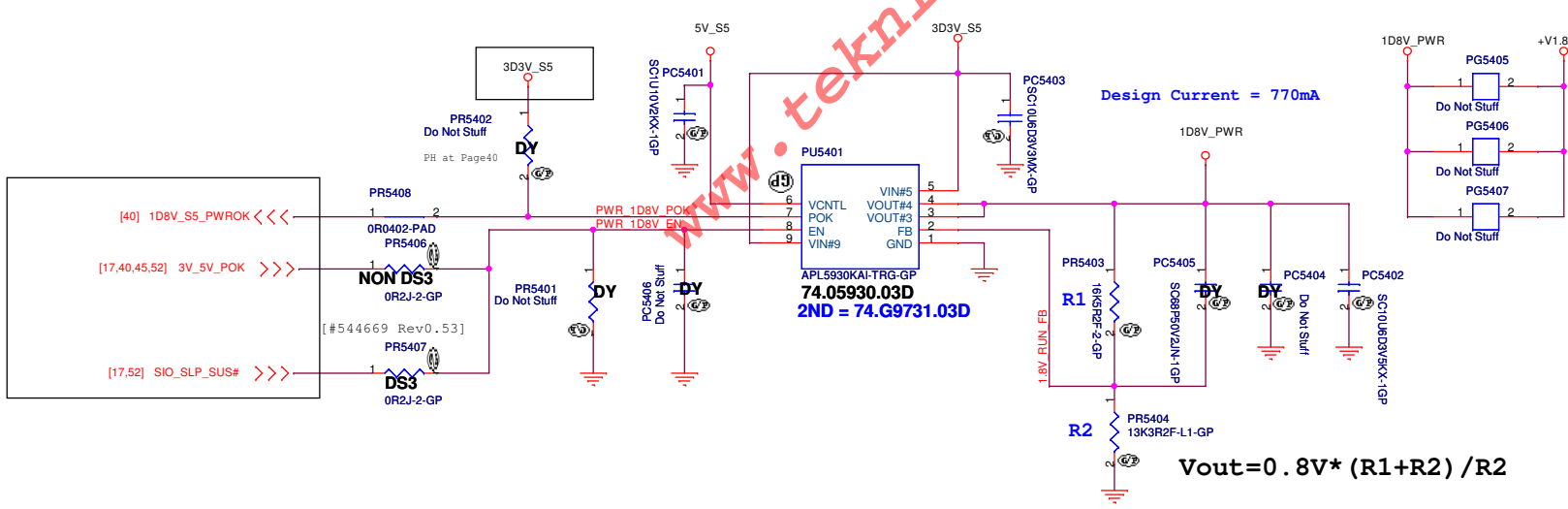
APL5930 for 2D5V

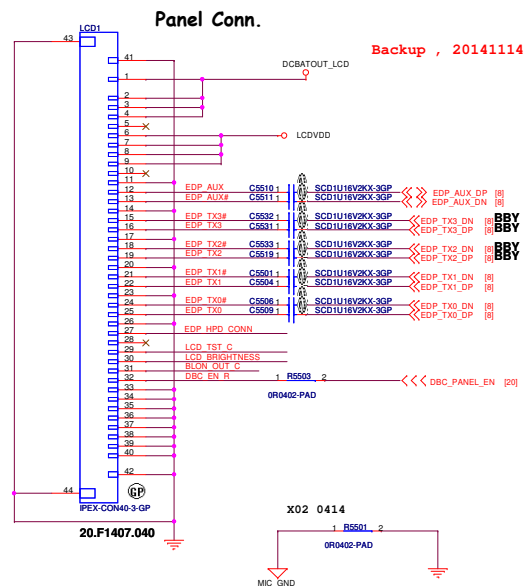


S-1339D15-M5001 for 1D5V_S0



APL5930 for 1D8V_S5

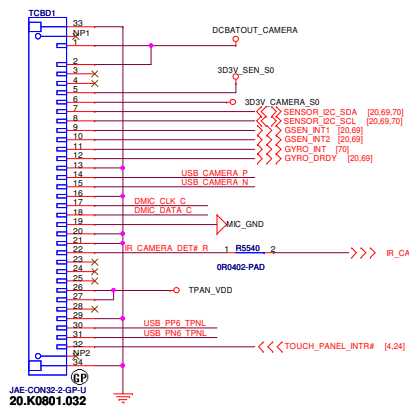
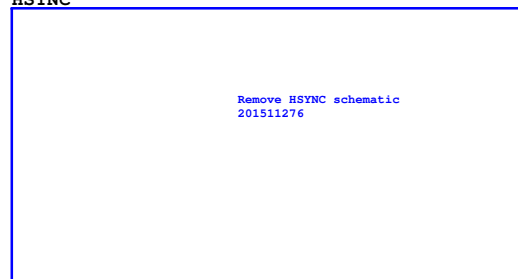




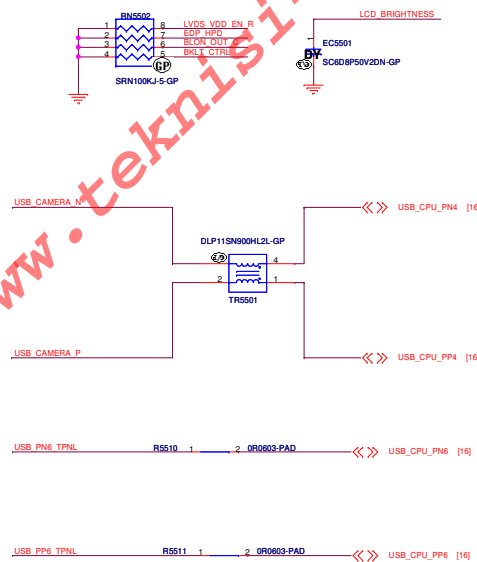
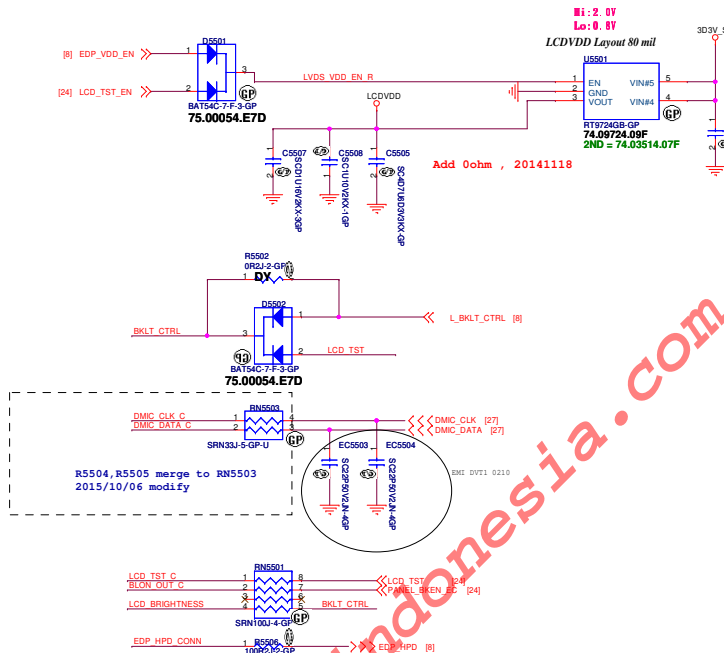
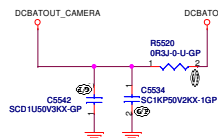
Power Pin Count : 7

GND Pin Count : 9

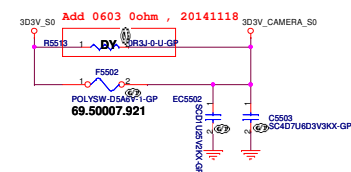
HSYNC



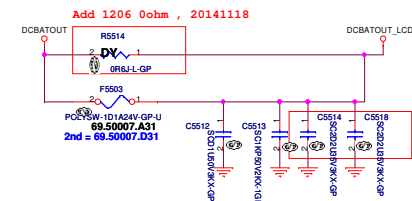
IR CAMERA Power



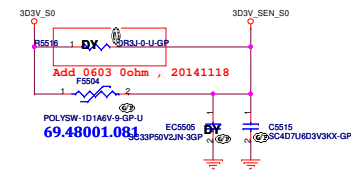
CAMERA POWER



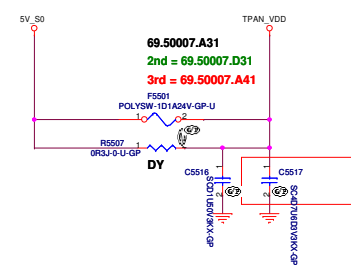
INVERTER POWER

Starload height limite change to 0603 package
2015/09/24 modify

SENSOR POWER




TOUCH PANEL POWER

Starload height limite change to 0603 package
2015/09/30 modify

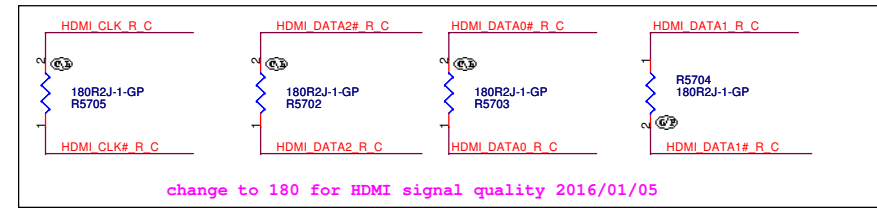
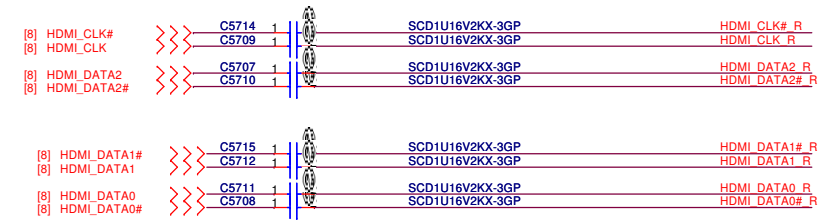
DVT2 03/24

-Core Design-

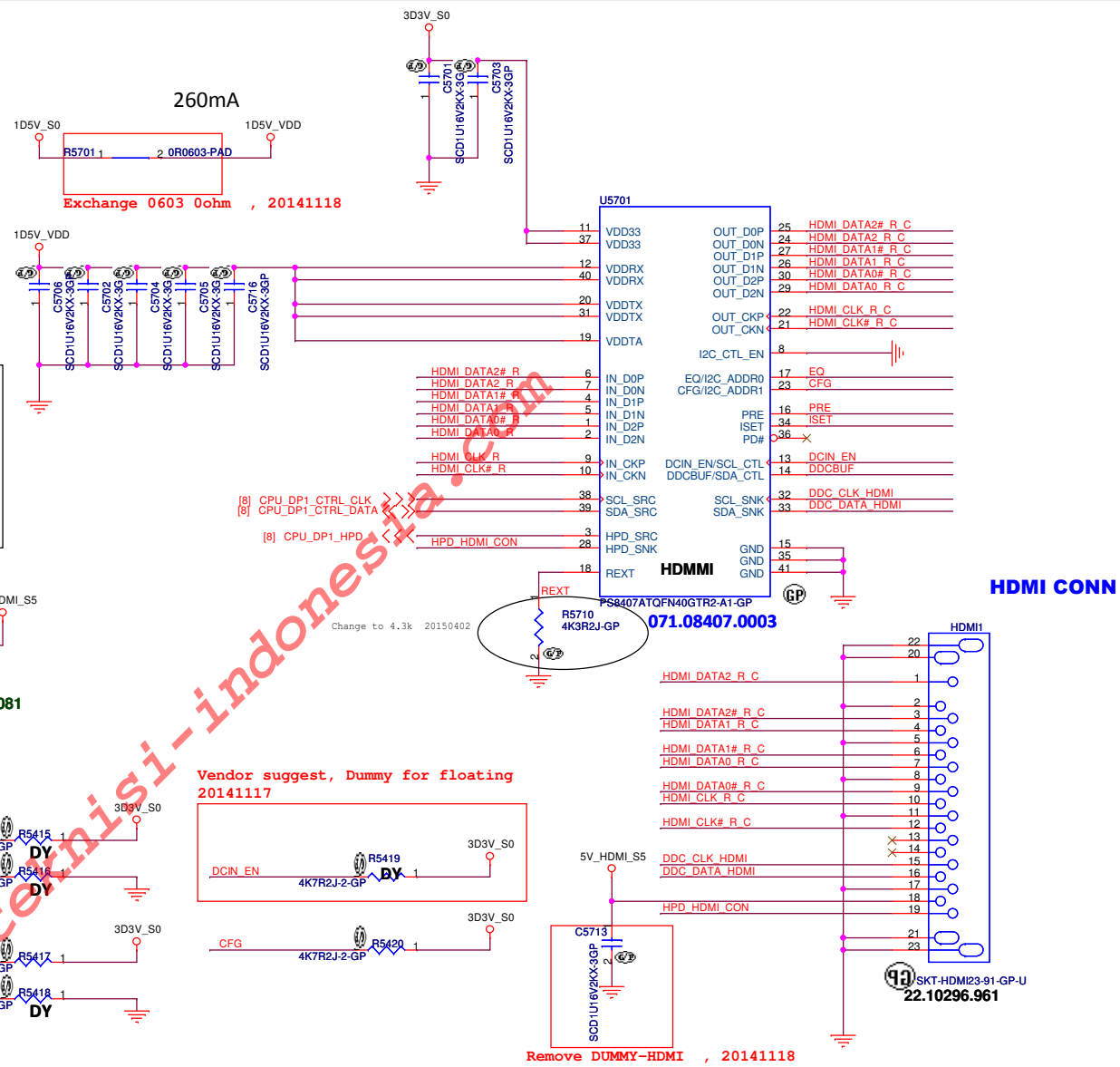
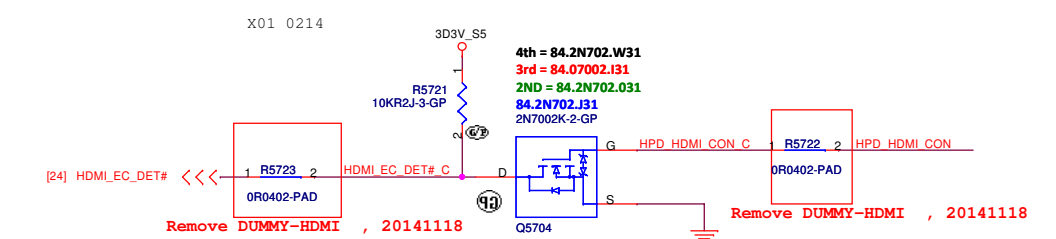
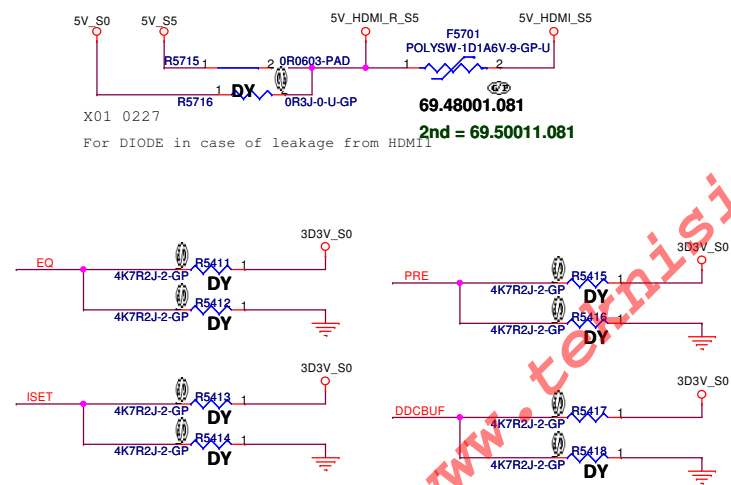
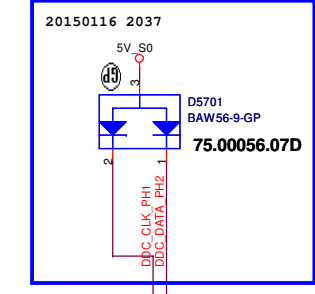
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Title CRT		
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Main Func = HDMI




Change symbol part number, because origin symbol is DELL OBS part



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Size

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Size

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Main Func = WLAN

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Title

NGFF WLAN CONN


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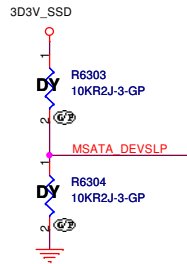
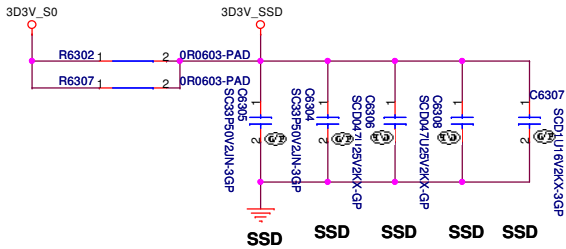
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number Starload SKL-U		Rev A00
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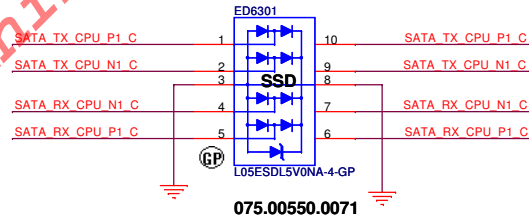
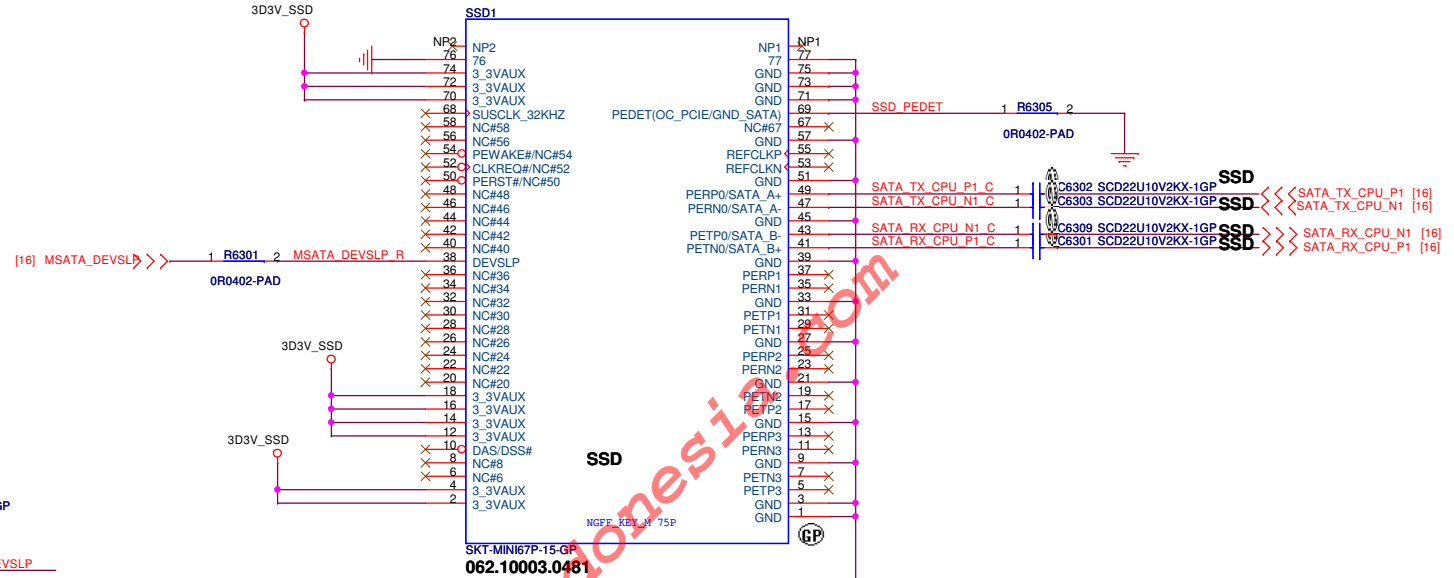
SSD M.2

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.



SSD M.2 CONN



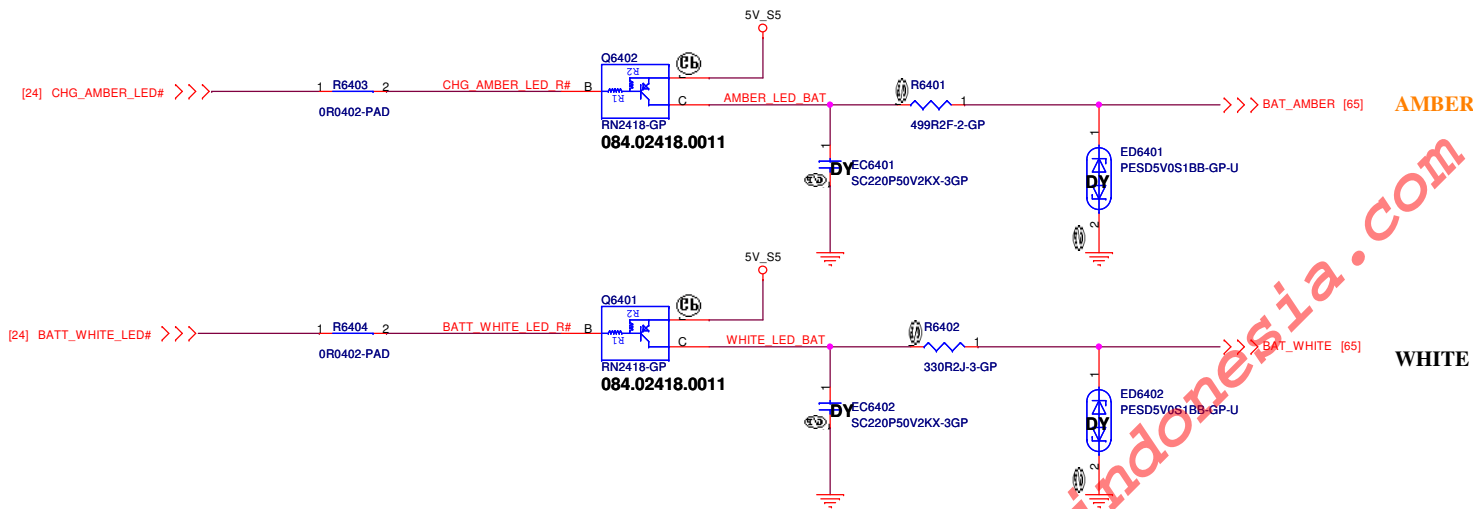
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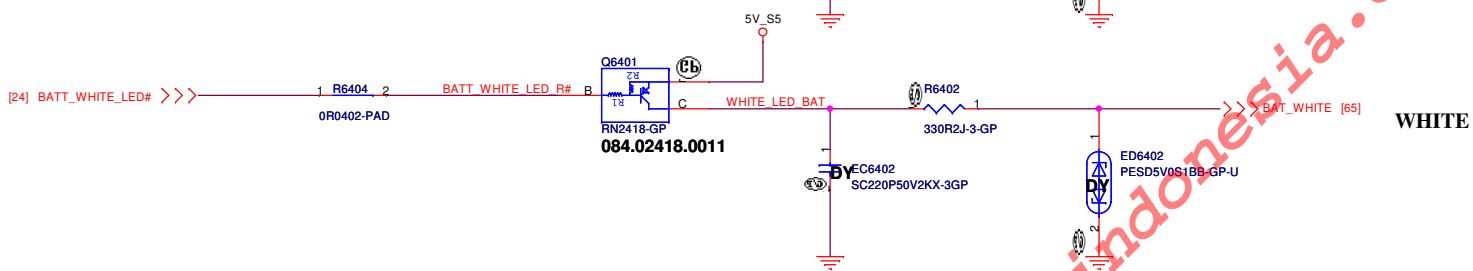
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Title			(Reserved)
Size	Document Number	Rev	
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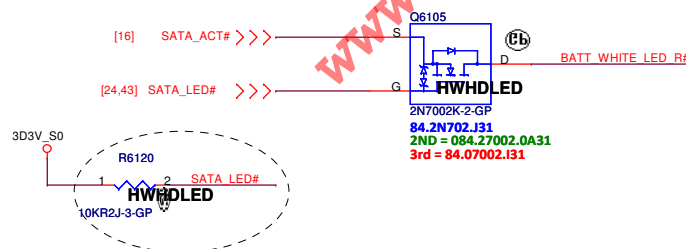
Battery LED1 (AMBER_LED)
Low activated from KBC GPIO



Battery LED2 (WHITE_LED)
Low activated from KBC GPIO

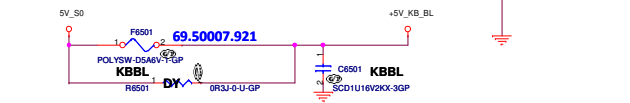
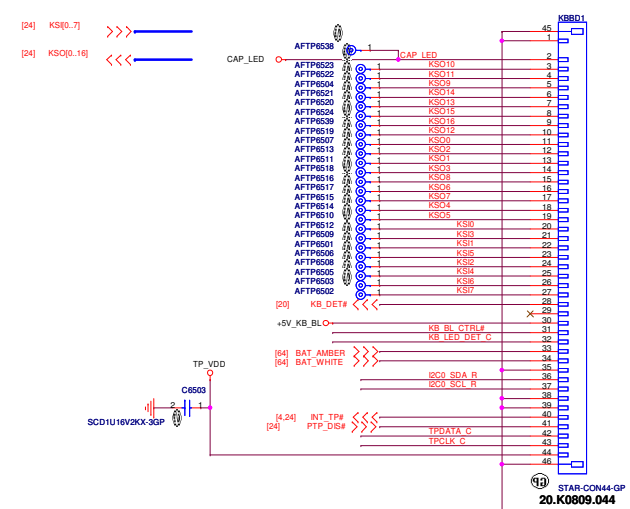


SATA LED

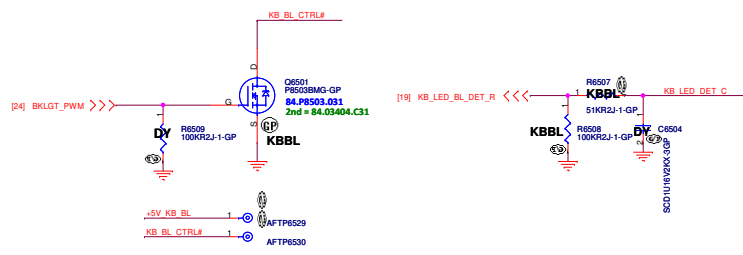


Add SATA LED solution by customer request 2016/02/03

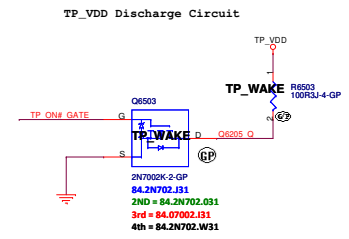
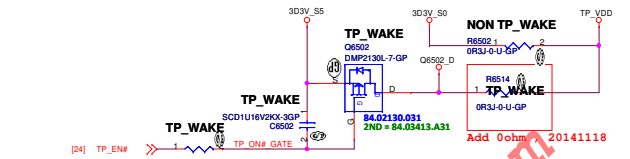
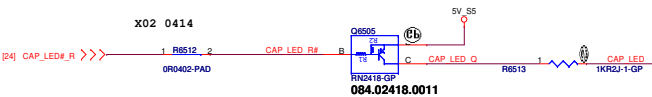
Keyboard



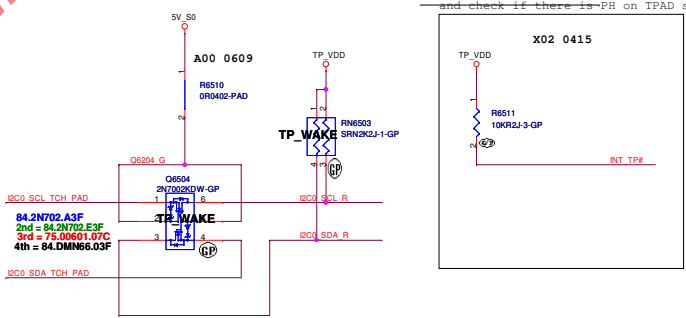
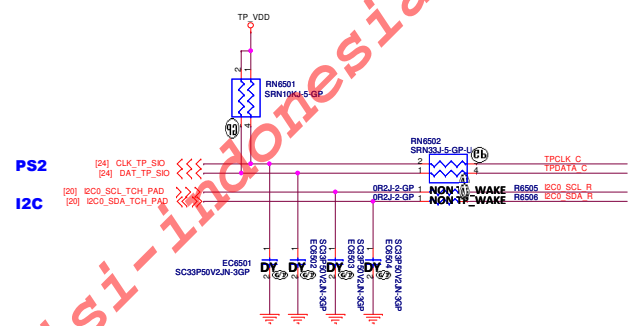
KB Backlight Power Consumption: 285mA max.



CAP LED Control
LOW active from KBC GPIO

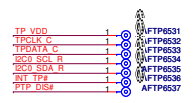


GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

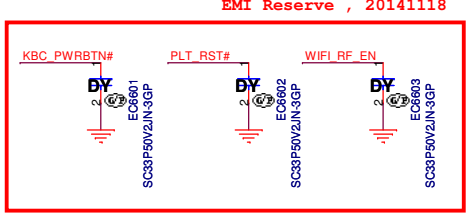
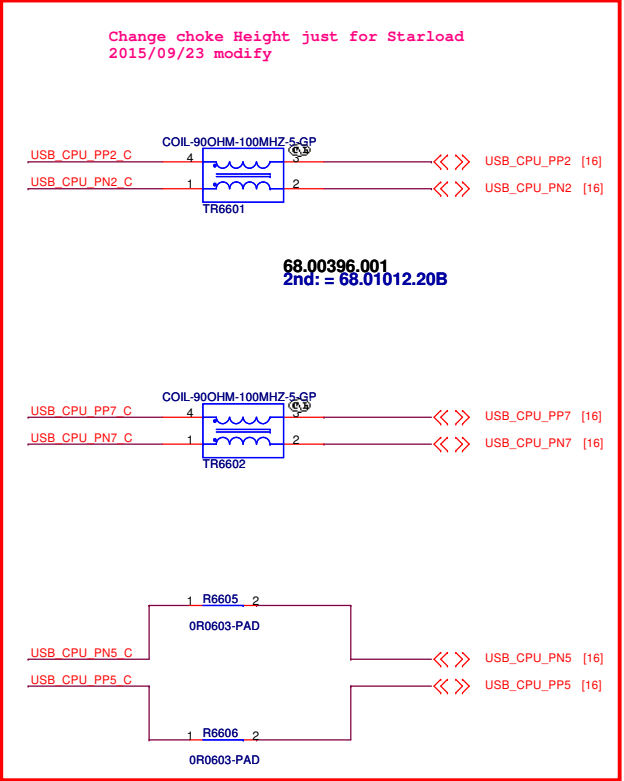
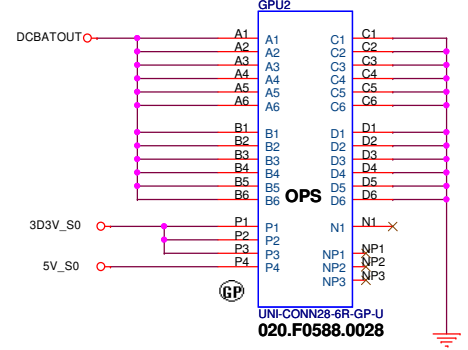
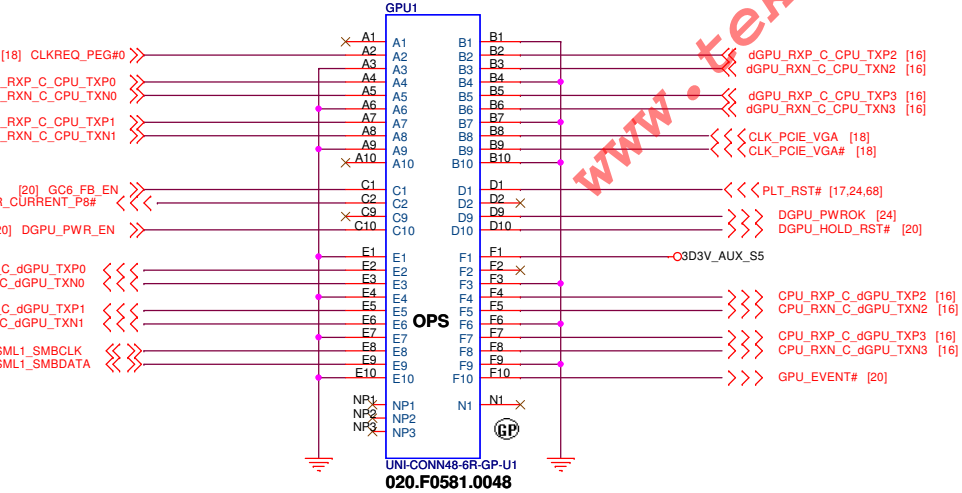
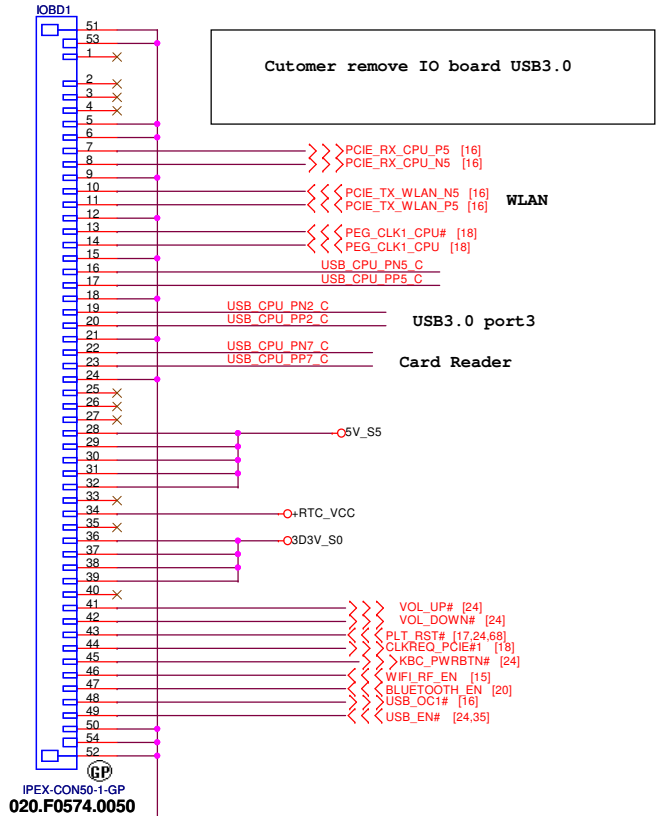


Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)



Main Func = IO Connector



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Title: **IO Board Connector**


Size: A3 Document Number: **Starload SKL-U** Rev: **A00**

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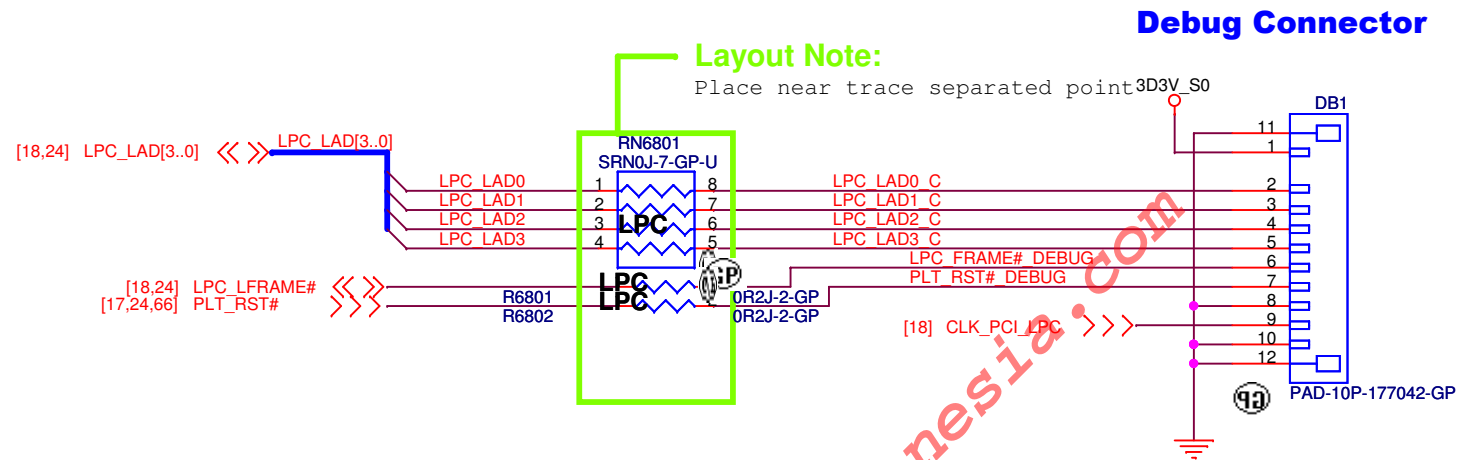
Rev

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Main Func = Debug



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

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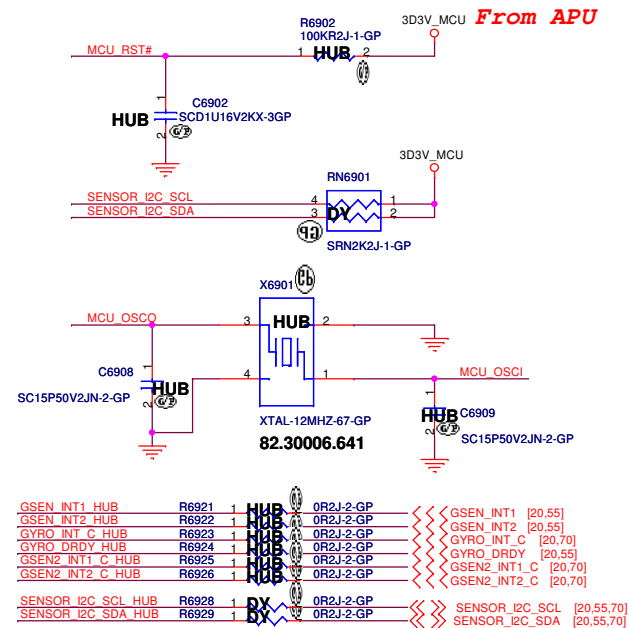
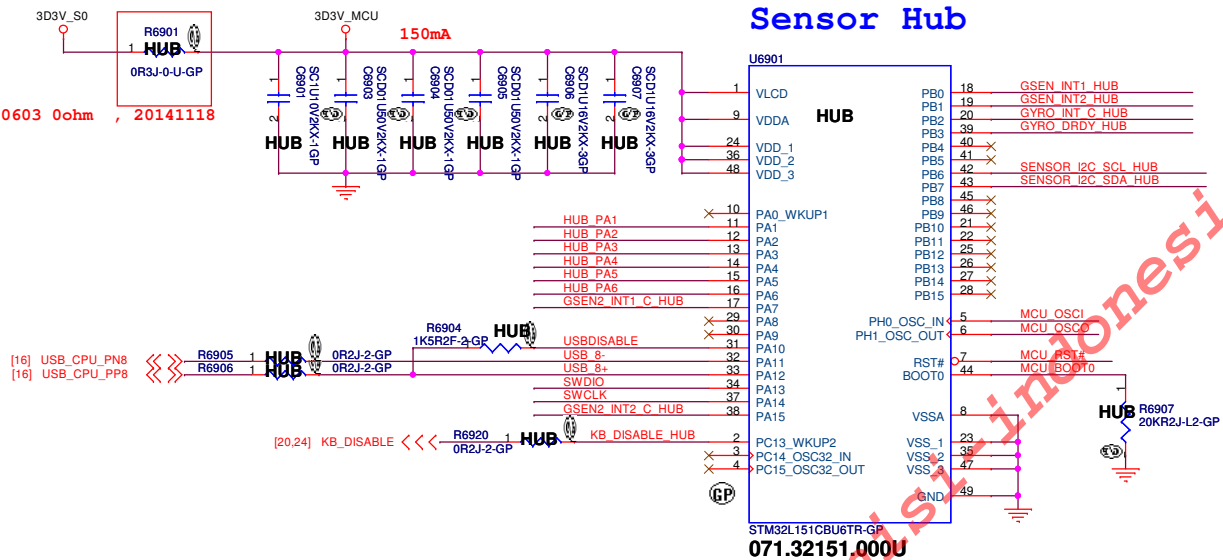
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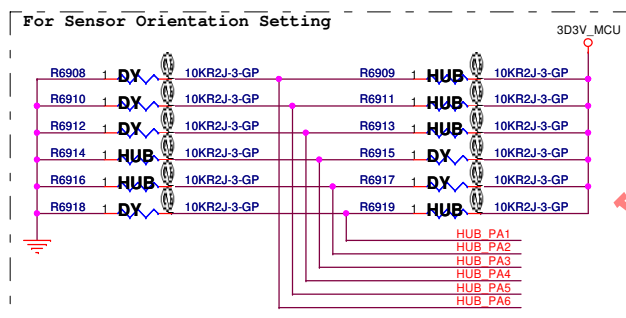
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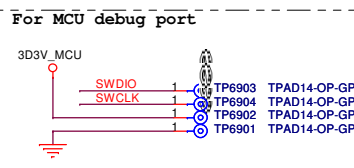
change 0603 0ohm , 20141118



For Sensor Orientation Setting



For MCU debug port



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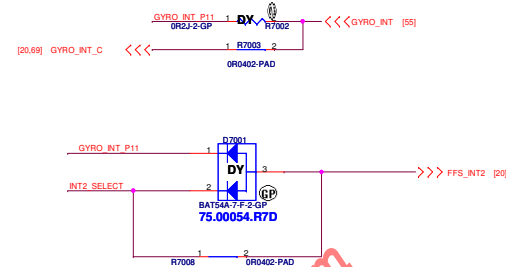
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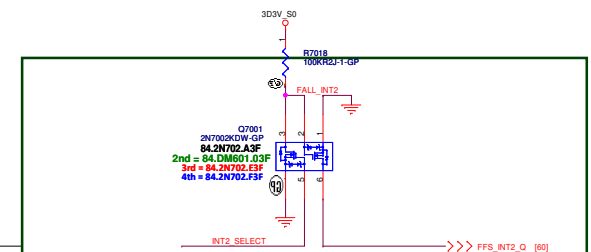
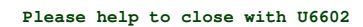
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combine G



- **Note:**
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can




Note:

- (1) Keep all signals are the same trace width. (included VDD, GND)
- (2) No VIA under IC bottom.

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Main Func = dGPU

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GPU(5/5)PWR/GND

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GPU-VRAM1,2 (1/4)

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GPU-VRAM3,4 (2/4)

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GPU-VRAM5,6 (3/4)

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GPU-VRAM7,8 (4/4)

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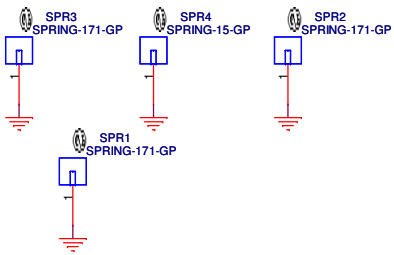
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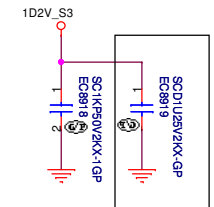
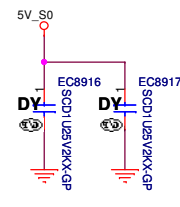
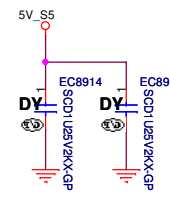
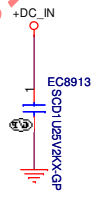
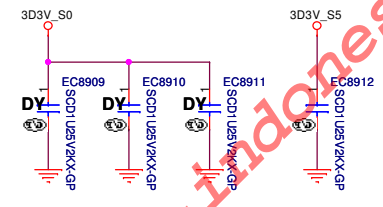
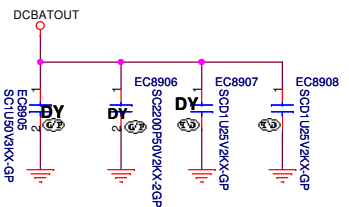
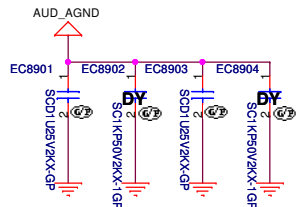
Main Func = UnusedParts

34.4YW18.001



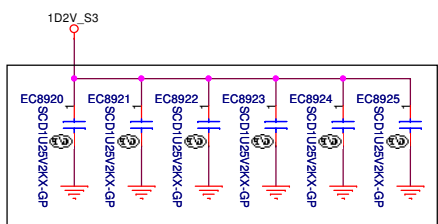
SSID = EMI

Mind the voltage rating of the caps.

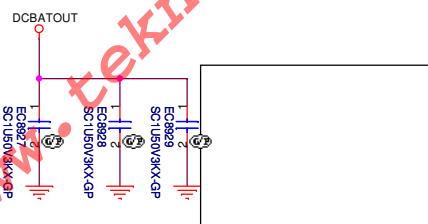


Change to 0.1uF at 20150427 for EMI

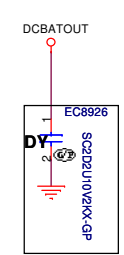
SSID = RF



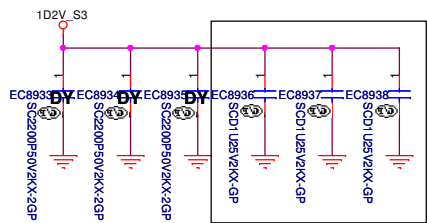
Change to 0.1uF at 20150427 for EMI



Remove EC8931,EC8932,EC8926,EC8930for placement



RF request 2016/01/12 modify




Change to 0.1uF at 20150427 for EMI

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SSID = TPM

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CRT Switch

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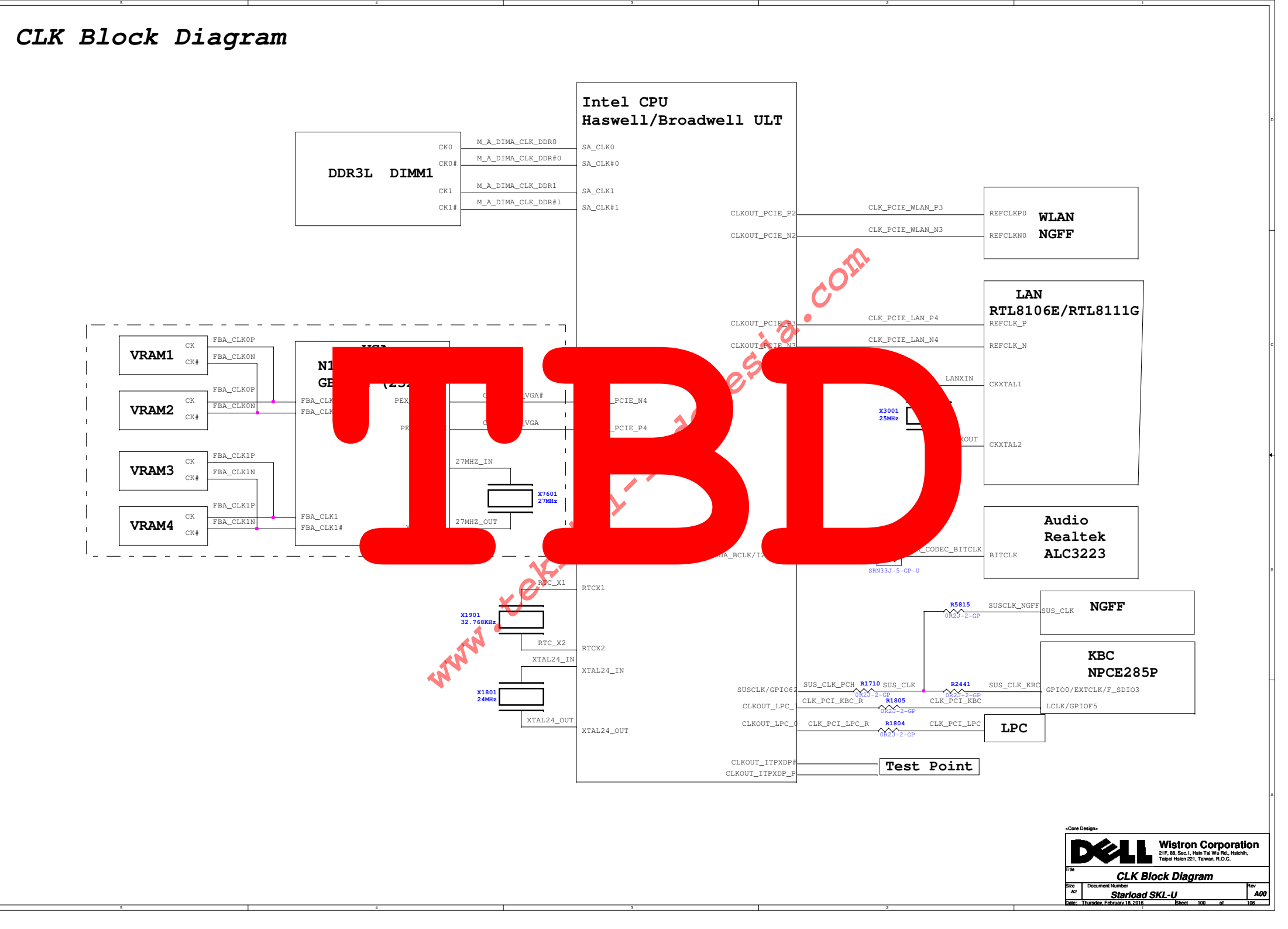
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```
Main Func = Debug
```

The CLK Block Diagram illustrates the clock distribution architecture for a system. Key components and their connections include:

- Intel CPU Haswell/Broadwell ULT**: The central processing unit, connected to various clock signals like SA_CLK0, SA_CLK#0, SA_CLK1, and SA_CLK#1.
- DDR3L DIMM1**: Connected to the CPU via M_A_DIMA_CLK_DDR0, M_A_DIMA_CLK_DDR#0, M_A_DIMA_CLK_DDR1, and M_A_DIMA_CLK_DDR#1.
- VRAM1, VRAM2, VRAM3, VRAM4**: Connected to the CPU via FBA_CLKOP, FBA_CLKON, FBA_CLK1P, FBA_CLK1N, FBA_CLK1, and FBA_CLK1#.
- N1 GE**: Connected to the CPU via PE# and PE#.
- LAN (RTL8106E/RTL8111G)**: Connected to the CPU via LANXIN and LANXOUT.
- WLAN (NGFF)**: Connected to the CPU via REFCLKP0, REFCLKN0, and CLKOUT_PCIE_P2.
- Audio (Realtek ALC3223)**: Connected to the CPU via BITCLK and SUSCLK_NGFF.
- KBC (NPCE285P)**: Connected to the CPU via GPI00/EXTCLK/F_SDIO3 and LCLK/GPI0F5.
- LPC**: Connected to the CPU via CLKOUT_LPC_0, CLKOUT_LPC_1, and CLKOUT_LPC_2.
- Test Point**: Connected to the CPU via CLKOUT_ITPXPDP# and CLKOUT_ITPXPDP_P.

The diagram also shows various clock signals and their frequencies, such as 27MHz, 32.768KHz, 24MHz, and 25MHz. A large red watermark "TBD" is overlaid on the diagram.



[illegible]

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[illegible]

The timing diagram shows three digital signals over time. The signals are labeled 2D5V_S3, 1D2V_S3, and 0D6V_S0. All three signals transition from a low state to a high state at the same time. The signal 2D5V_S3 is the top trace, 1D2V_S3 is the middle trace, and 0D6V_S0 is the bottom trace. The transitions are simultaneous and occur at a specific point in time.

Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 enter and exit sequence and timing requirements.

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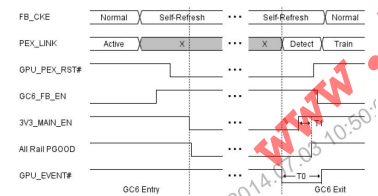


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

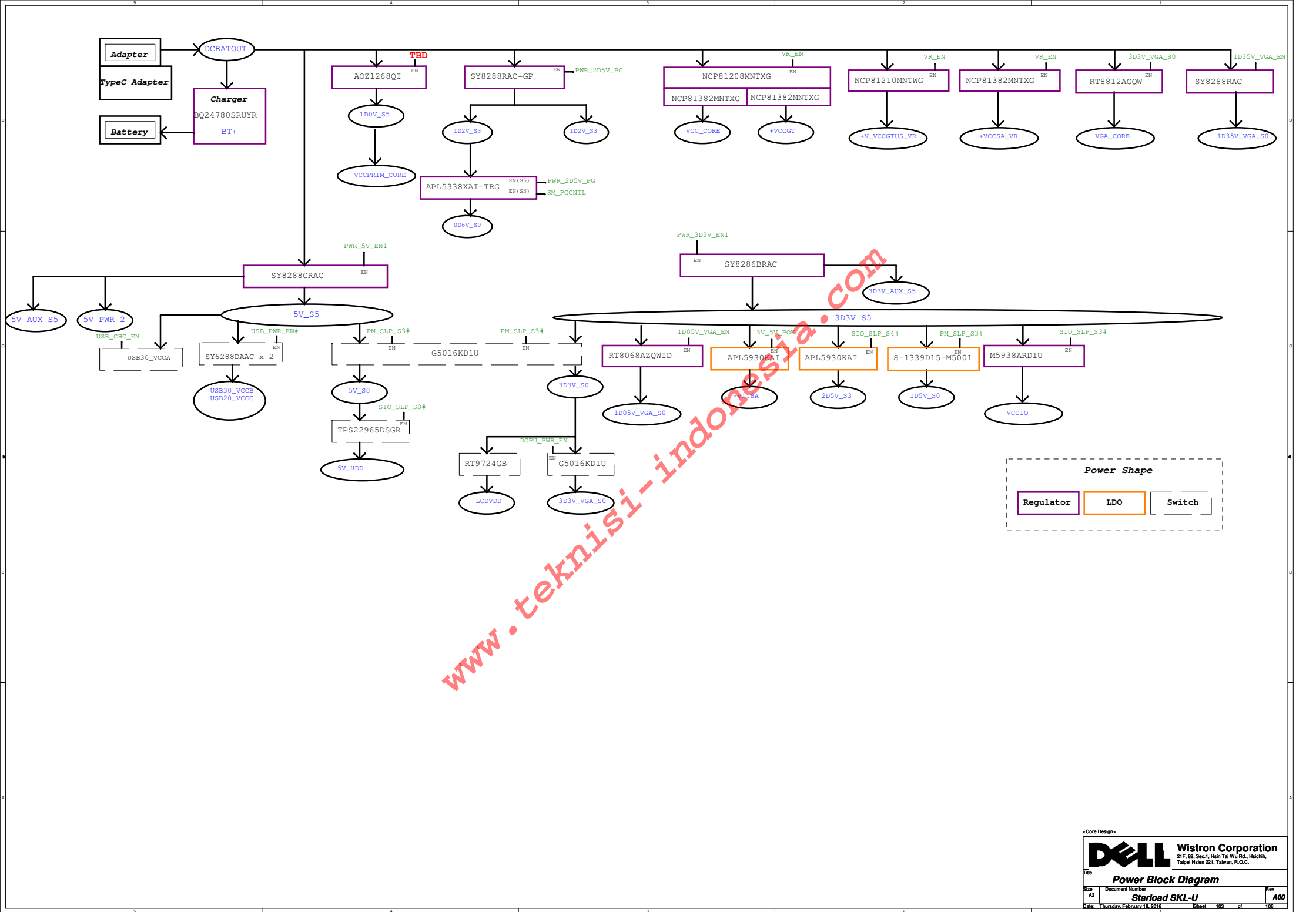
Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

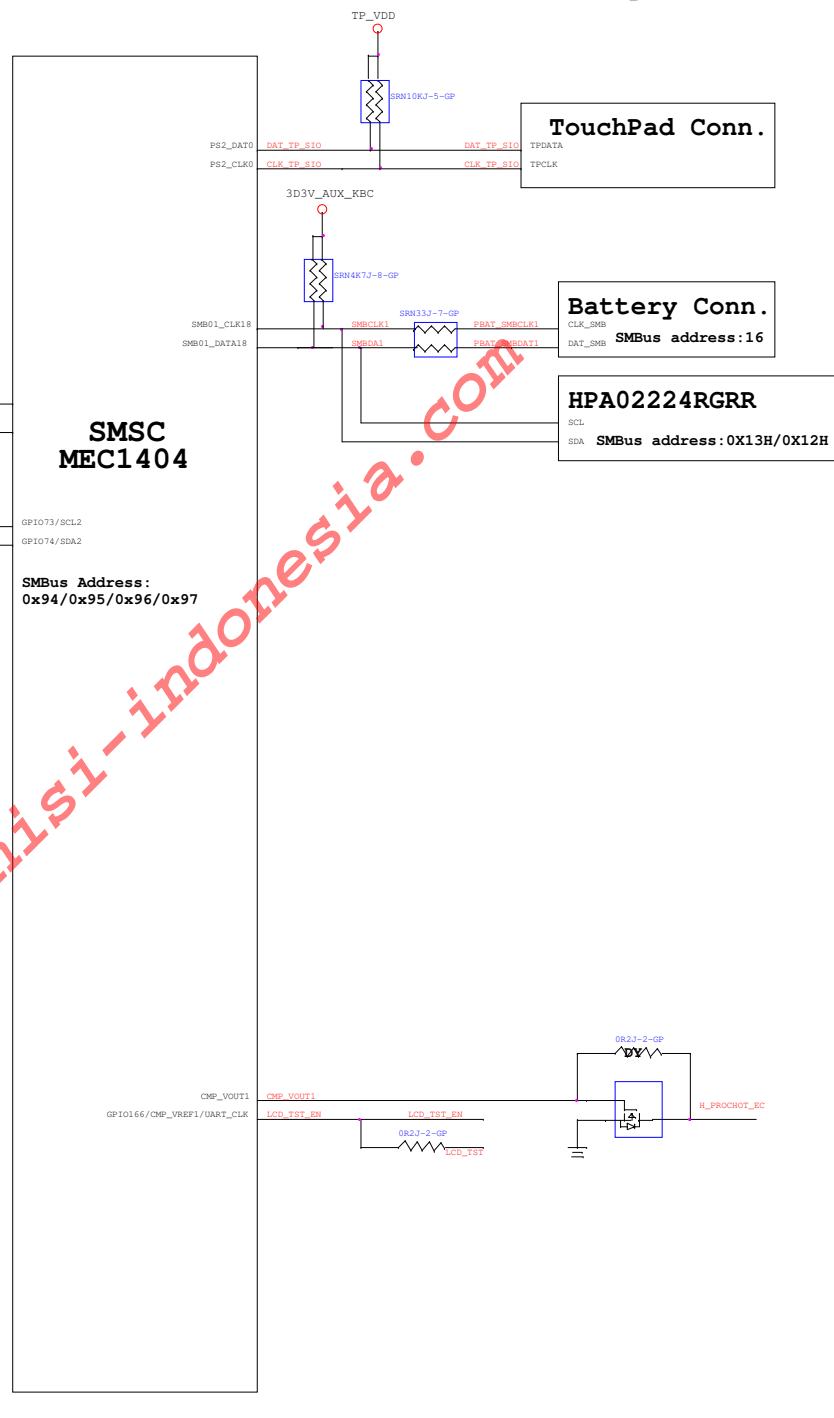
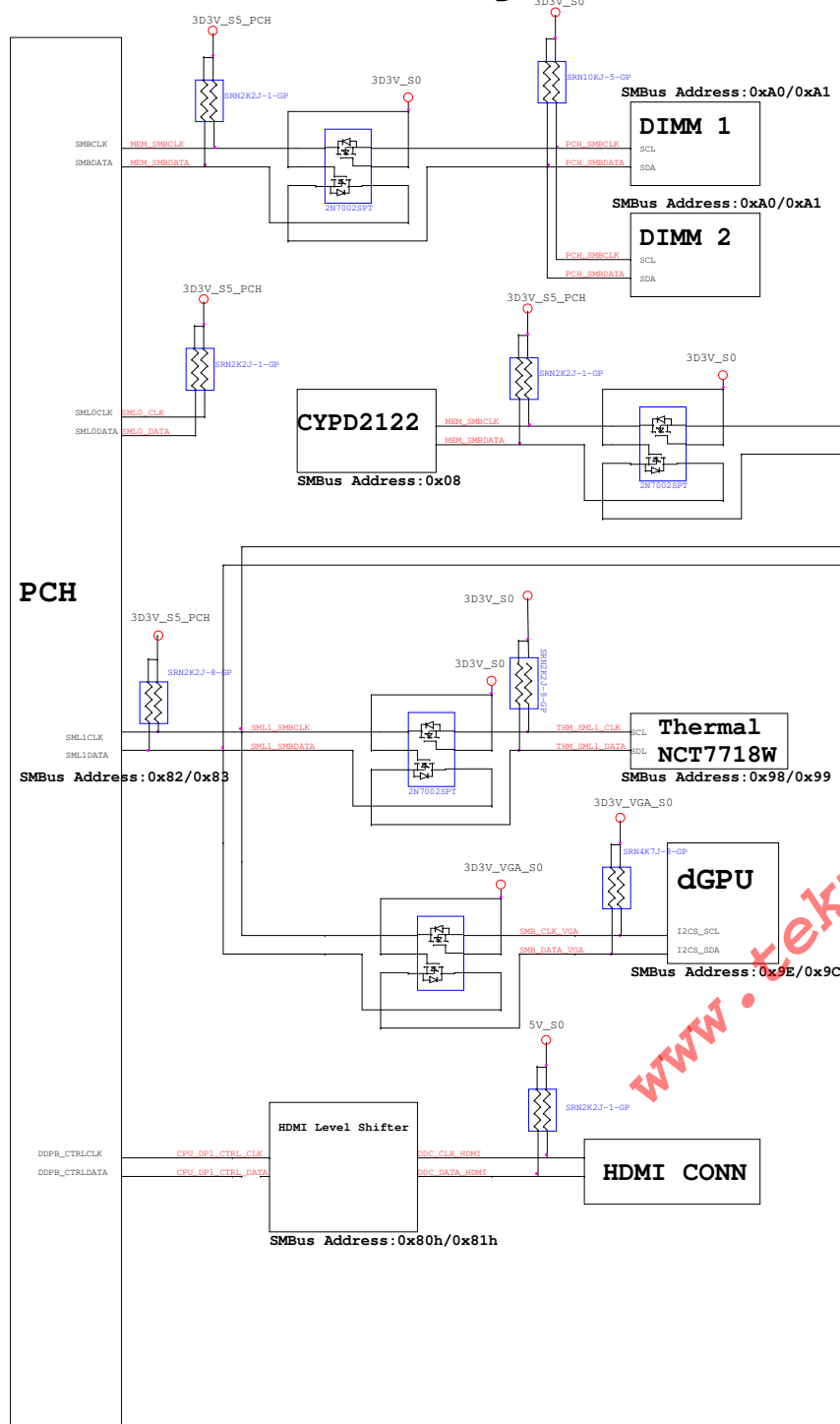
- ALL Rail PGOOD#1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During G6x exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/G stays on.
- All delays should be minimized to increase time spent in G6x for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.



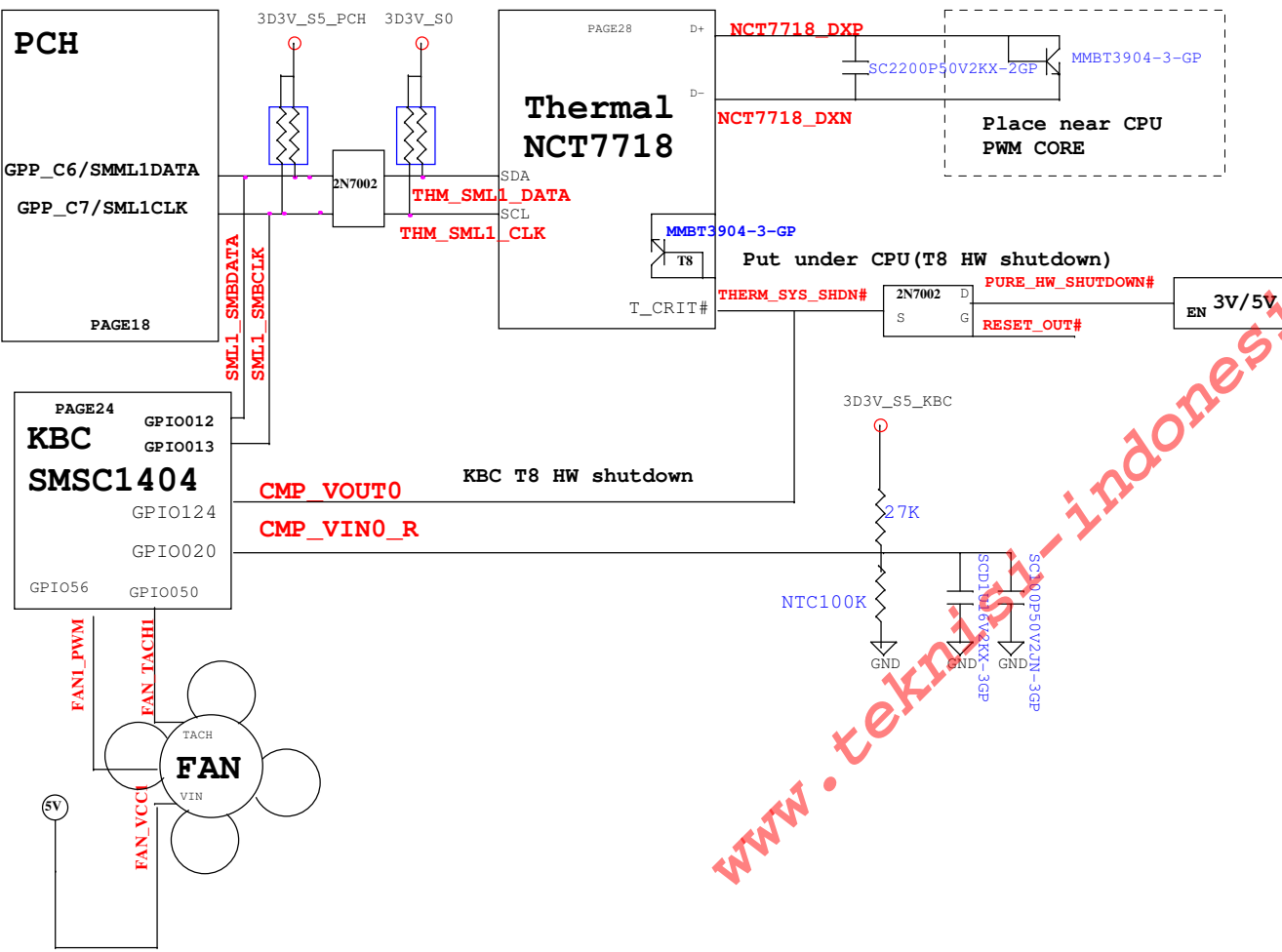


PCH SMBus Block Diagram

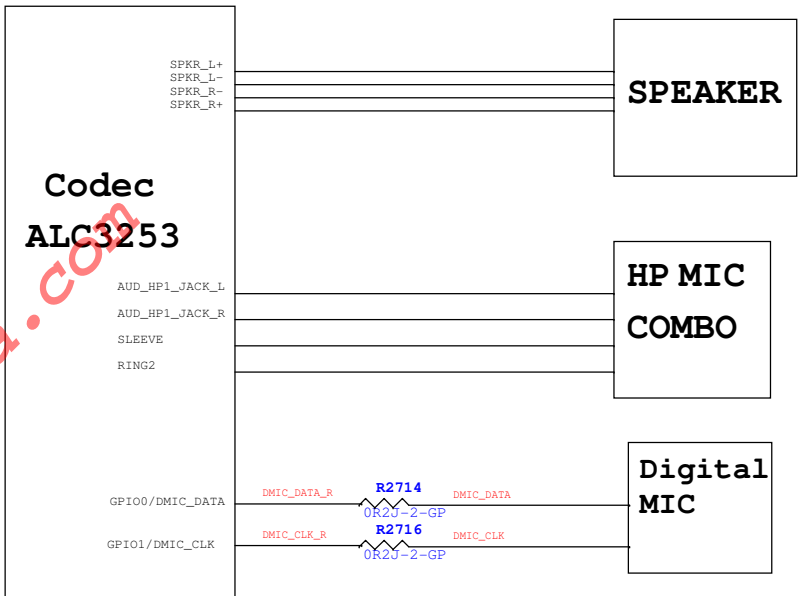
KBC SMBus Block Diagram



Thermal Block Diagram




Audio Block Diagram



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